LDL08E13A

LDLABO

2008 年 6 月 14 日

第 1 章

論理譜

```
{ ========================================================================= }
{    LCD ドライバ                                                          }
{ ========================================================================= }
logicname LDL08E13A

{ ========================================================================= }
{    実効譜                                                                }
{ ========================================================================= }
entity main
{ ------------------------------------------------------------------------- }
{    入力                                                                  }
{ ------------------------------------------------------------------------- }
input  RESET;
input  CLKIN;
input  ADATA[4];
input  BDATA[4];
input  ACK;

{ ------------------------------------------------------------------------- }
{    出力                                                                  }
{ ------------------------------------------------------------------------- }
output A1S;
output B1S;
output C1S;
output D1S;
output E1S;
output F1S;
output G1S;
output A2S;
output B2S;
output C2S;
output D2S;
output E2S;
output F2S;
output G2S;
output COM;

{ ------------------------------------------------------------------------- }
{    内部信号                                                              }
{ ------------------------------------------------------------------------- }
bitn a1s;
bitn b1s;
bitn c1s;
bitn d1s;
bitn e1s;
bitn f1s;
bitn g1s;
```

```
bitn a2s;
bitn b2s;
bitn c2s;
bitn d2s;
bitn e2s;
bitn f2s;
bitn g2s;

bitr acseq;
bitr count[4];
bitr clkp[2];
bitr adata[4];
bitr bdata[4];
bitn ack;

{ ------------------------------------------------------------------------ }
{    入力代入                                                              }
{ ------------------------------------------------------------------------ }
   ack=!ACK;

{ ------------------------------------------------------------------------ }
{    出力代入                                                              }
{ ------------------------------------------------------------------------ }
   COM=!acseq;

   if (acseq)
      A1S=a1s;
      B1S=b1s;
      C1S=c1s;
      D1S=d1s;
      E1S=e1s;
      F1S=f1s;
      G1S=g1s;
   else
      A1S=!a1s;
      B1S=!b1s;
      C1S=!c1s;
      D1S=!d1s;
      E1S=!e1s;
      F1S=!f1s;
      G1S=!g1s;
   endif

   if (acseq)
      A2S=a2s;
      B2S=b2s;
      C2S=c2s;
      D2S=d2s;
      E2S=e2s;
      F2S=f2s;
      G2S=g2s;
   else
      A2S=!a2s;
      B2S=!b2s;
      C2S=!c2s;
      D2S=!d2s;
      E2S=!e2s;
      F2S=!f2s;
      G2S=!g2s;
   endif

{ ------------------------------------------------------------------------ }
{    データ A                                                              }
{ ------------------------------------------------------------------------ }
   if (RESET)
```

```
      adata=0;
   else
      if (ack)
         adata=ADATA;
      else
         adata=adata;
      endif
   endif

{ ------------------------------------------------------------------------ }
{    データ B                                                             }
{ ------------------------------------------------------------------------ }
   if (RESET)
      bdata=0;
   else
      if (ack)
         bdata=BDATA;
      else
         bdata=bdata;
      endif
   endif

{ ------------------------------------------------------------------------ }
{    LCDCOM                                                               }
{ ------------------------------------------------------------------------ }
   acseq=count.3;

{ ------------------------------------------------------------------------ }
{    LCD 駆動 CLK 立ち上がり                                              }
{ ------------------------------------------------------------------------ }
   if (RESET)
      clkp=0;
   else
      switch(clkp)
         case 0: if (CLKIN) clkp=1; endif
         case 1: clkp=2;
         case 2:
            if (CLKIN) clkp=clkp; else clkp=0; endif
      endswitch
   endif

{ ------------------------------------------------------------------------ }
{    LCD 駆動 CLK 計数                                                    }
{ ------------------------------------------------------------------------ }
   if (RESET)
      count=0;
   else
      if (clkp.0)
         count=count+1;
      else
         count=count;
      endif
   endif

{ ------------------------------------------------------------------------ }
{    LCD 出力 A                                                           }
{ ------------------------------------------------------------------------ }
   switch(adata)
      case 0:
               a1s=1;
               b1s=1;
               c1s=1;
               d1s=1;
               e1s=1;
               f1s=1;
```

```
        g1s=0;
case 1:
        a1s=0;
        b1s=1;
        c1s=1;
        d1s=0;
        e1s=0;
        f1s=0;
        g1s=0;
case 2:
        a1s=1;
        b1s=1;
        c1s=0;
        d1s=1;
        e1s=1;
        f1s=0;
        g1s=1;
case 3:
        a1s=1;
        b1s=1;
        c1s=1;
        d1s=1;
        e1s=0;
        f1s=0;
        g1s=1;
case 4:
        a1s=0;
        b1s=1;
        c1s=1;
        d1s=0;
        e1s=0;
        f1s=1;
        g1s=1;
case 5:
        a1s=1;
        b1s=0;
        c1s=1;
        d1s=1;
        e1s=0;
        f1s=1;
        g1s=1;
case 6:
        a1s=1;
        b1s=0;
        c1s=1;
        d1s=1;
        e1s=1;
        f1s=1;
        g1s=1;
case 7:
        a1s=1;
        b1s=1;
        c1s=1;
        d1s=0;
        e1s=0;
        f1s=0;
        g1s=0;
case 8:
        a1s=1;
        b1s=1;
        c1s=1;
        d1s=1;
        e1s=1;
        f1s=1;
        g1s=1;
case 9:
```

```
                a1s=1;
                b1s=1;
                c1s=1;
                d1s=0;
                e1s=0;
                f1s=1;
                g1s=1;
        endswitch

{ ------------------------------------------------------------------------ }
{     LCD 出力 B                                                          }
{ ------------------------------------------------------------------------ }
    switch(bdata)
        case 0:
                a2s=1;
                b2s=1;
                c2s=1;
                d2s=1;
                e2s=1;
                f2s=1;
                g2s=0;
        case 1:
                a2s=0;
                b2s=1;
                c2s=1;
                d2s=0;
                e2s=0;
                f2s=0;
                g2s=0;
        case 2:
                a2s=1;
                b2s=1;
                c2s=0;
                d2s=1;
                e2s=1;
                f2s=0;
                g2s=1;
        case 3:
                a2s=1;
                b2s=1;
                c2s=1;
                d2s=1;
                e2s=0;
                f2s=0;
                g2s=1;
        case 4:
                a2s=0;
                b2s=1;
                c2s=1;
                d2s=0;
                e2s=0;
                f2s=1;
                g2s=1;
        case 5:
                a2s=1;
                b2s=0;
                c2s=1;
                d2s=1;
                e2s=0;
                f2s=1;
                g2s=1;
        case 6:
                a2s=1;
                b2s=0;
                c2s=1;
                d2s=1;
```

```
                e2s=1;
                f2s=1;
                g2s=1;
        case 7:
                a2s=1;
                b2s=1;
                c2s=1;
                d2s=0;
                e2s=0;
                f2s=1;
                g2s=0;
        case 8:
                a2s=1;
                b2s=1;
                c2s=1;
                d2s=1;
                e2s=1;
                f2s=1;
                g2s=1;
        case 9:
                a2s=1;
                b2s=1;
                c2s=1;
                d2s=0;
                e2s=0;
                f2s=1;
                g2s=1;
        endswitch

ende
```

```
{ ========================================================================== }
{    機能実行譜                                                            }
{ ========================================================================== }
entity sim
{ -------------------------------------------------------------------------- }
{    端子                                                                  }
{ -------------------------------------------------------------------------- }
output RESET;
output CLKIN;
output ADATA[4];
output BDATA[4];
output ACK;
output A1S;
output B1S;
output C1S;
output D1S;
output E1S;
output F1S;
output G1S;
output A2S;
output B2S;
output C2S;
output D2S;
output E2S;
output F2S;
output G2S;
output COM;
input  simres;

{ -------------------------------------------------------------------------- }
{    内部信号                                                              }
{ -------------------------------------------------------------------------- }
bitr tc[8];

{ -------------------------------------------------------------------------- }
{    実効譜導入                                                            }
{ -------------------------------------------------------------------------- }
   part main(RESET,CLKIN,ADATA,BDATA,ACK
            ,A1S,B1S,C1S,D1S,E1S,F1S,G1S
            ,A2S,B2S,C2S,D2S,E2S,F2S,G2S
            ,COM
            )

{ -------------------------------------------------------------------------- }
{    検査位置計数                                                          }
{ -------------------------------------------------------------------------- }
   if (!simres) tc=tc+1; endif

{ -------------------------------------------------------------------------- }
{    初期化                                                                }
{ -------------------------------------------------------------------------- }
   if (tc<5) RESET=1; endif

{ -------------------------------------------------------------------------- }
{    データ確定                                                            }
{ -------------------------------------------------------------------------- }
   switch(tc)
      case 10: ACK=0;
      default: ACK=1;
   endswitch

{ -------------------------------------------------------------------------- }
{    LCD 駆動 CLK                                                          }
```

```
{ ------------------------------------------------------------------------ }
   CLKIN=tc.0;

{ ------------------------------------------------------------------------ }
{    データ                                                  }
{ ------------------------------------------------------------------------ }
   ADATA=1;
   BDATA=2;

ende

endlogic
```