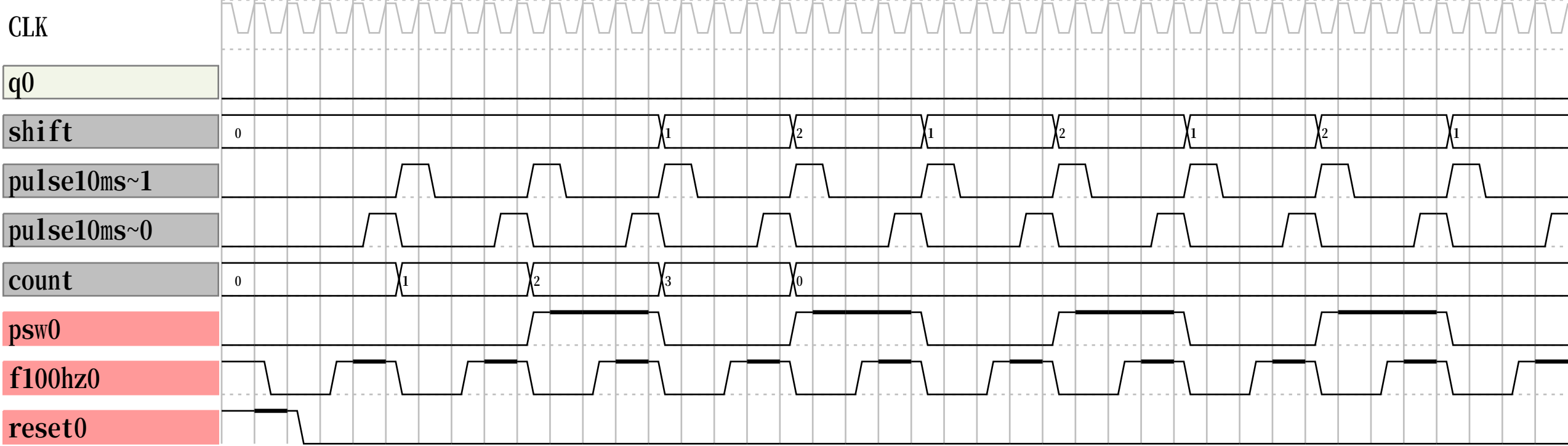
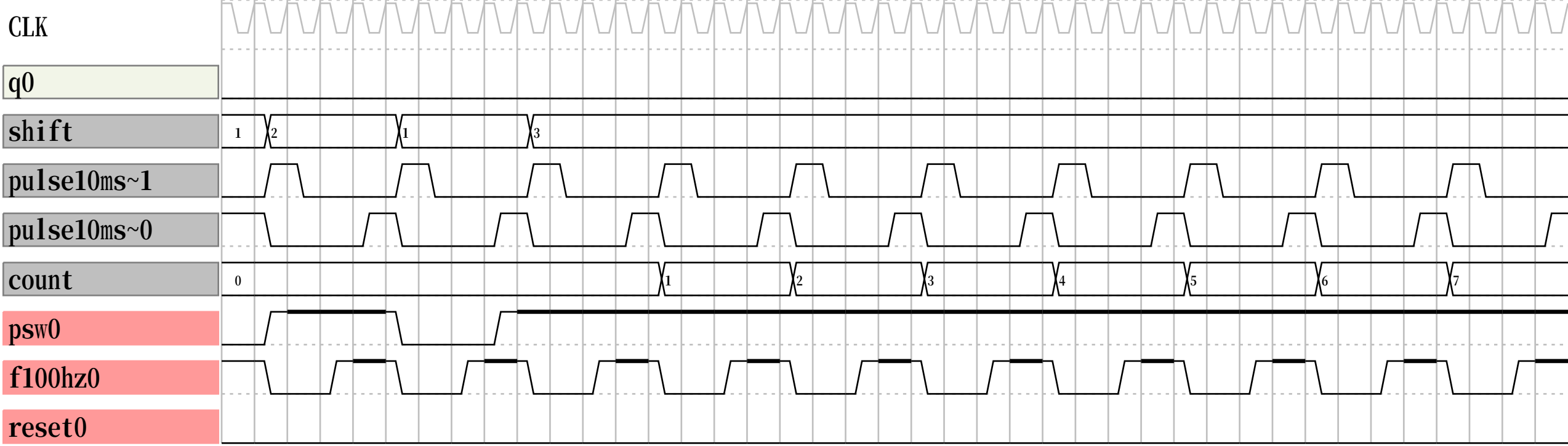
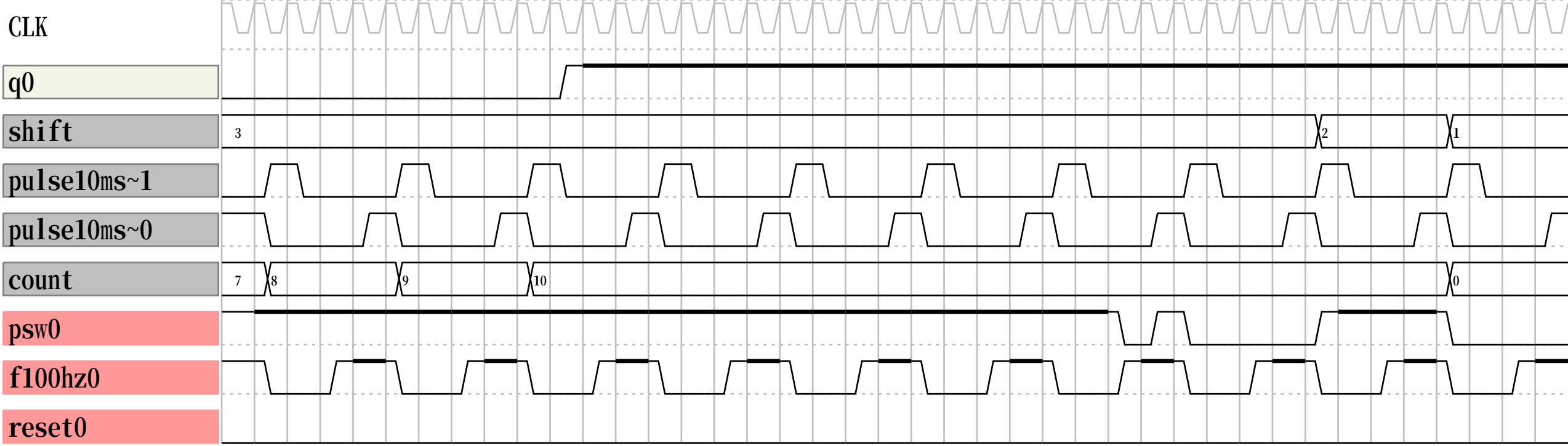
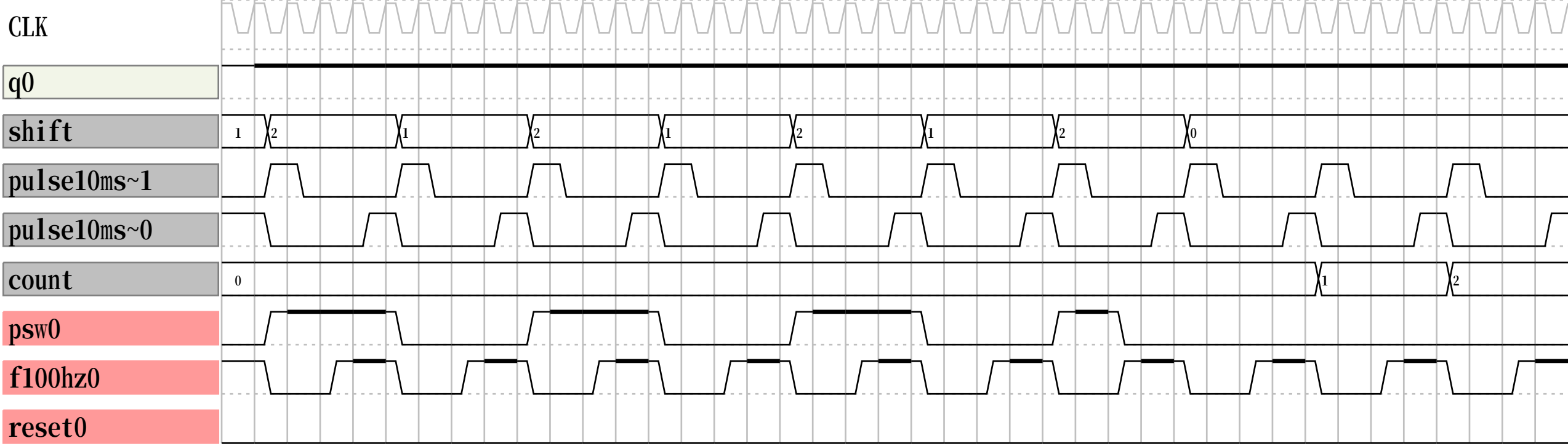

CLK
q0
shift
0
1
2
1
2
1
2
1
pulse10ms~1
pulse10ms~0
count
0
1
2
3
0
psw0
f100hz0
reset0


CLK
q0
shift
1
2
1
3
pulse10ms~1
pulse10ms~0
count
0
1
2
3
4
5
6
7
psw0
f100hz0
reset0

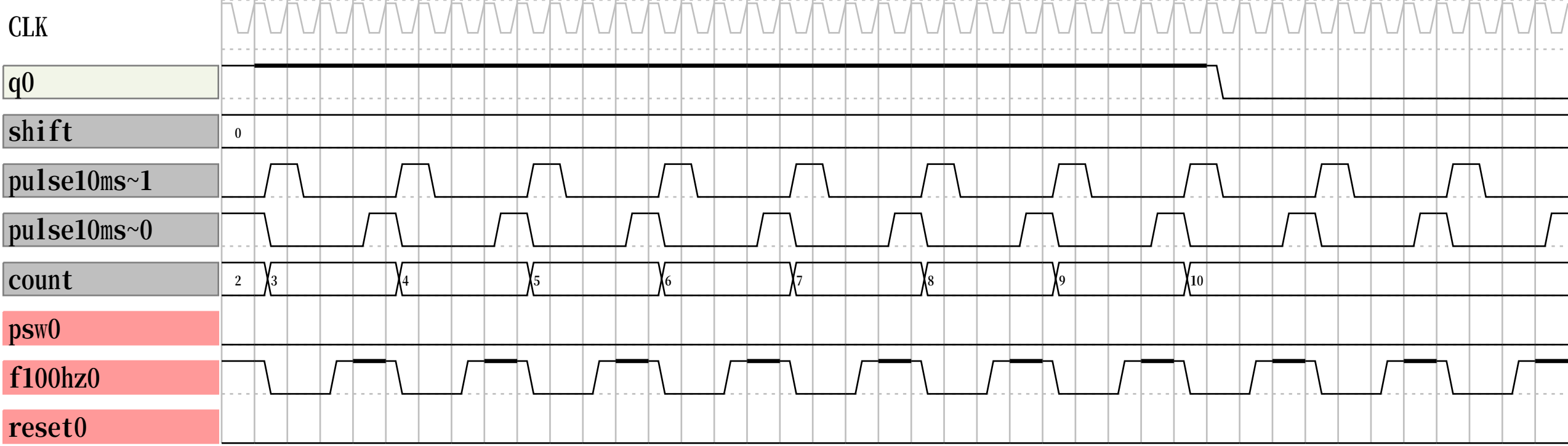
43 - 83 0 - 7 DEC


CLK
q0
shift
3
2
1
pulse10ms~1
pulse10ms~0
count
7
8
9
10
0
psw0
f100hz0
reset0

83 - 123 0 - 7 DEC



123 - 163 0 - 7 DEC


CLK
q0
shift
0
pulse10ms~1
pulse10ms~0
count
2
3
4
5
6
7
8
9
10
psw0
f100hz0
reset0