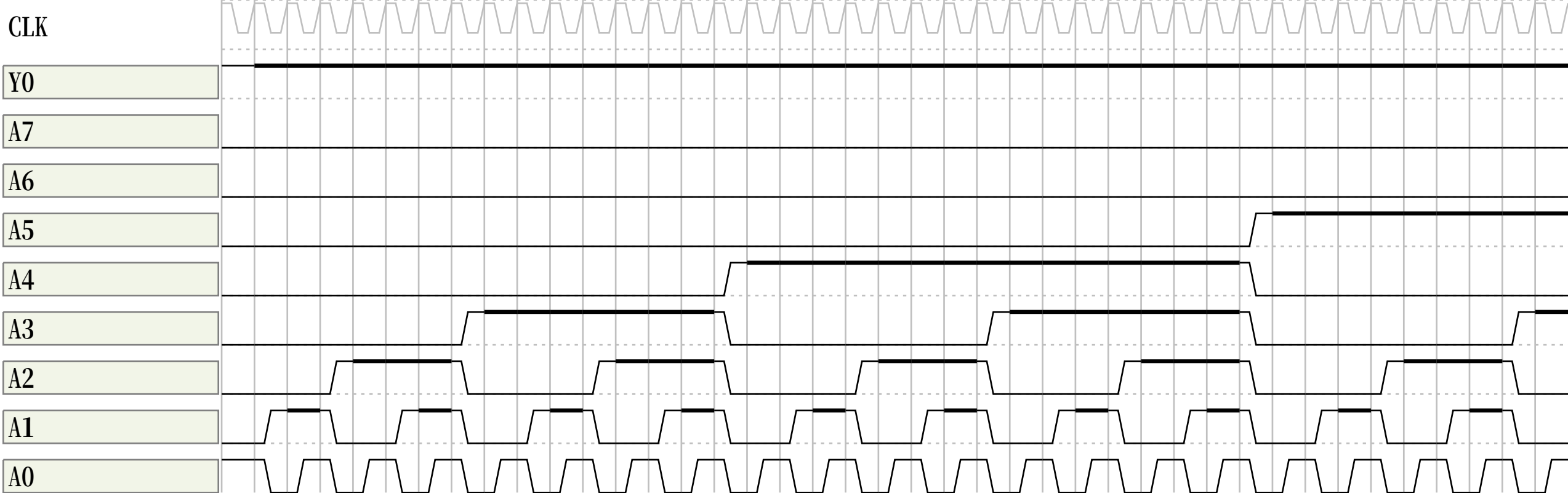
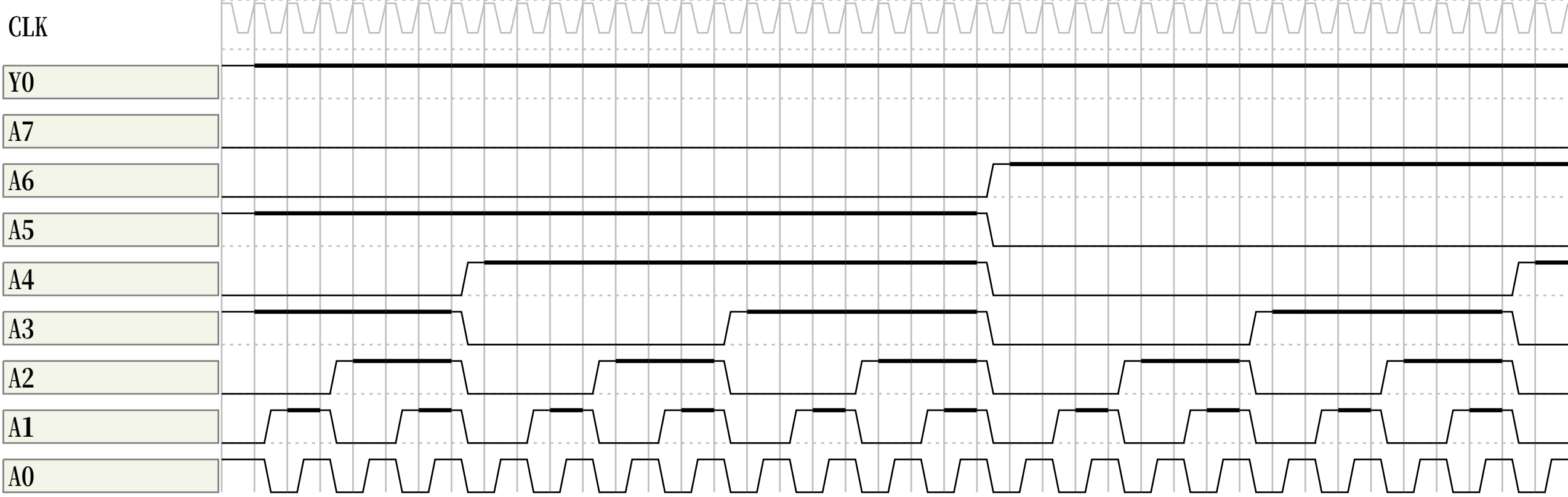
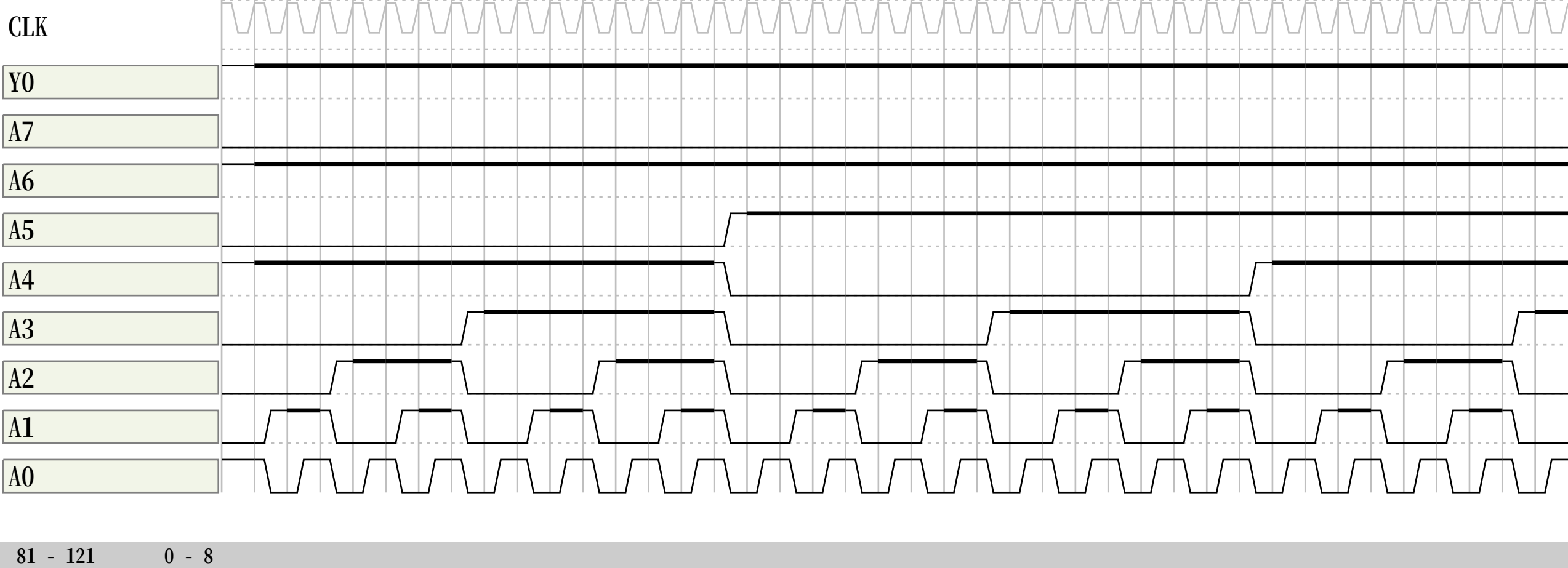
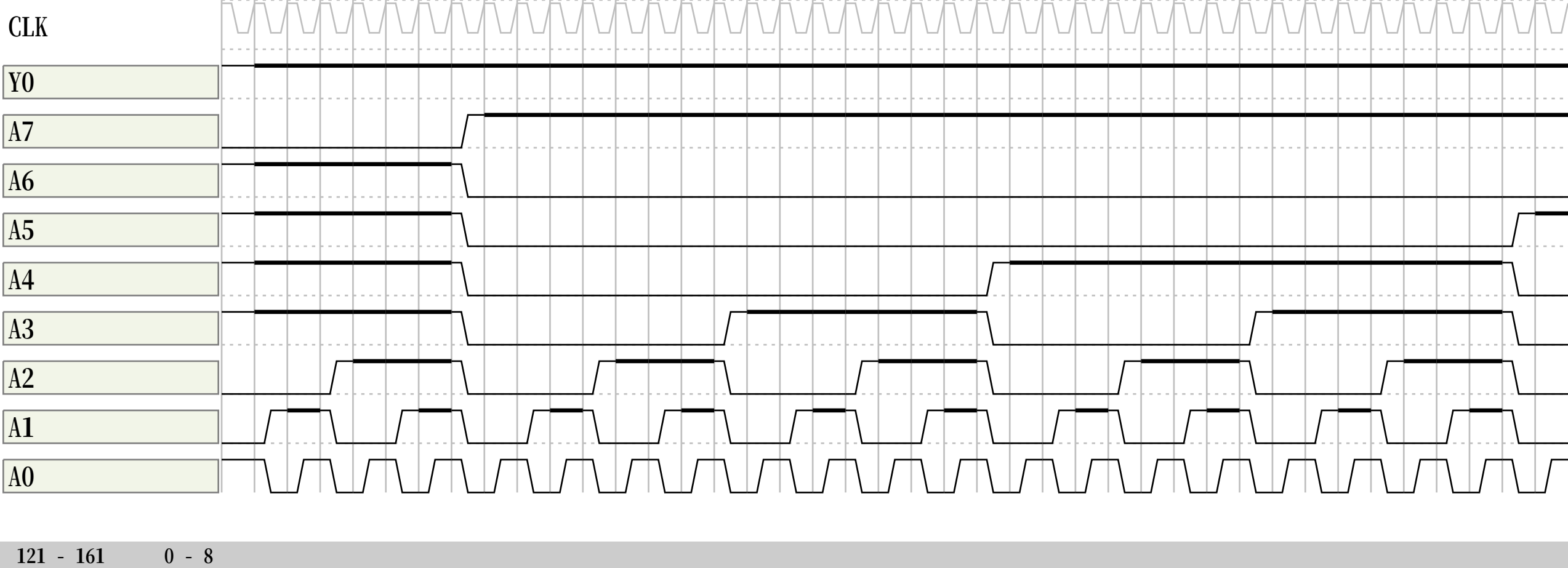










The timing diagram illustrates the operation of the 74161 4-bit binary counter. The clock (CLK) is a periodic square wave. The outputs Y0, A7, A6, A5, A4, A3, A2, A1, and A0 are shown as digital signals. The counter is shown in two states: 161 (00000001) and 201 (11001001). The output A0 is the least significant bit, and A7 is the most significant bit. The counter is shown in two states: 161 (00000001) and 201 (11001001).

Signal	161 - 201	0 - 8
CLK	High	High
Y0	Low	Low
A7	Low	Low
A6	Low	Low
A5	Low	Low
A4	Low	Low
A3	Low	Low
A2	Low	Low
A1	Low	Low
A0	Low	Low

