# LDL06E01D

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```
logicname LDL06E01D

entity main
input  RESET;
input  NP;
input  DATA[8];
output Q[8];

bitr q[8];

   Q=q;

   if (RESET)
      q=255;
   else
      if (NP)
         if (DATA<q)
            q=DATA;
         else
            q=q;
         endif
      else
         q=q;
      endif
   endif

ende

entity sim
output RESET;
output NP;
output DATA[8];
output Q[8];

bitr tc[8];

   part main(RESET,NP,DATA,Q)

   tc=tc+1;

   if (tc<5) RESET=1; endif

   switch(tc)
      case 10: NP=1; DATA=5;
      case 12: NP=1; DATA=4;
      case 14: NP=1; DATA=3;
      case 16: NP=1; DATA=2;
      case 18: NP=1; DATA=1;
      case 20: NP=1; DATA=6;
      case 22: NP=1; DATA=10;
      case 24: NP=1; DATA=7;
      case 26: NP=1; DATA=8;
      case 28: NP=1; DATA=9;
   endswitch

ende

endlogic
```

図 1　動作