# LDL06E02B

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```
logicname LDL06E02B

entity main
input  RESET;
input  EP;
input  DATA[8];
input  SEND;
output Q;
output BUSY;

bitr q[10];
bitr en;
bitr count[4];
bitr parity[4];
{
output T0P[4]; T0P=count;
output T1P[4]; T1P=parity;
}
   Q=q.0;
   BUSY=en;

   if (RESET)
      en=0;
   else
      if (SEND)
         en=1;
      else
         if (count==11)
            en=0;
         else
            en=en;
         endif
      endif
   endif

   if (RESET)
      count=0;
   else
      if (en)
         if (EP)
            count=count+1;
         else
            count=count;
         endif
      else
         count=0;
      endif
   endif

   if (RESET)
      parity=0;
   else
      if (en)
         if (count>1)
            if (EP)
               if (q.0)
                  parity=parity+1;
               else
                  parity=parity;
               endif
            else
               parity=parity;
            endif
         else
            parity=0;
         endif
      else
         parity=0;
      endif
   endif

   if (RESET|SEND)
      q.0=1;       { START BIT }
      q.2:9=DATA;  { DATA }
      q.10=1;      { STOP BIT }
   else
      if (en)
         if (EP)
            if (count==9)
               q.0=!parity.0;
               q.1:9=q.2:10;
            else
               q.0:9=q.1:10;
            endif
         else
            q=q;
         endif
      else
         q=q;
      endif
   endif

ende

entity sim
output RESET;
output EP;
```

```
output DATA[8];
output SEND;
output Q;
output BUSY;

bitr tc[8];

   part main(RESET,EP,DATA,SEND,Q,BUSY)

   tc=tc+1;

   if (tc<5) RESET=1; endif

   if (tc>50)
      DATA=0x25;
   else
      DATA=0x55;
   endif

   switch(tc)
      case 10: SEND=1;
      case 60: SEND=1;
   endswitch

   EP=tc.1:0==3;

ende

endlogic
```

図 1　動作 (1/3)

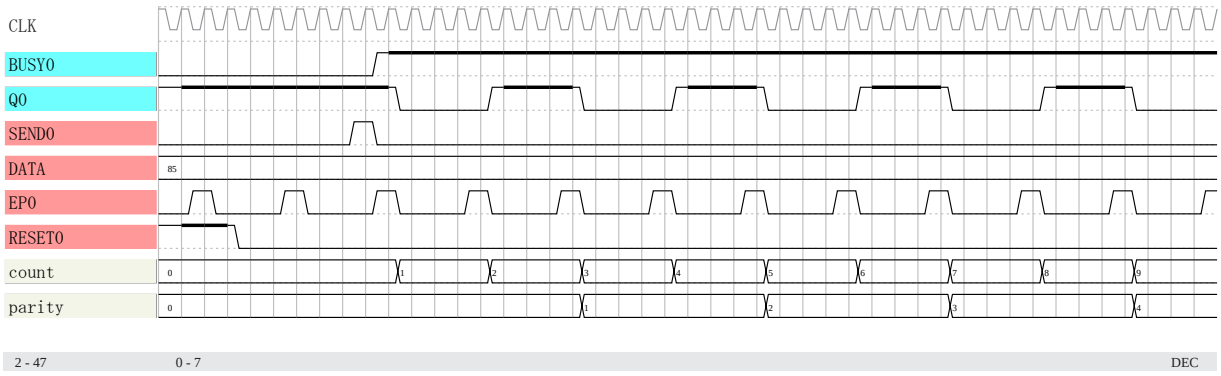



図 2　動作 (2/3)

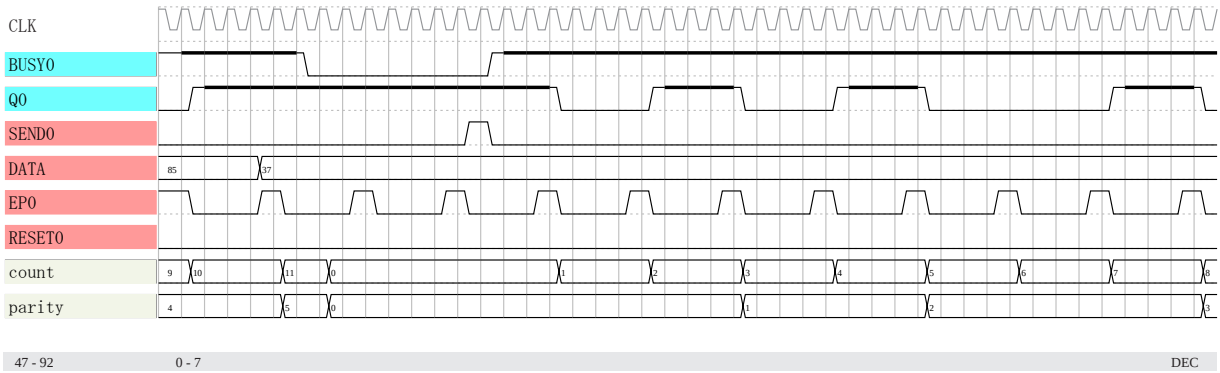
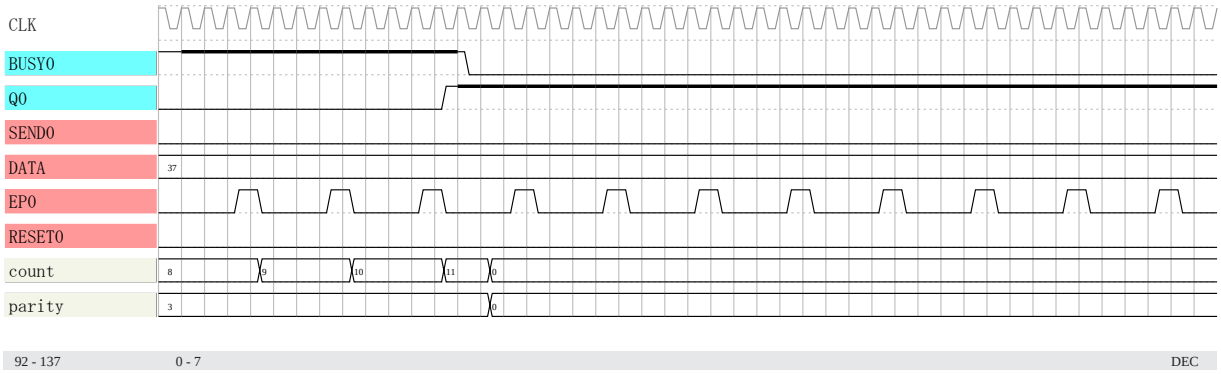


図 3　動作 (3/3)


CLK
BUSY0
Q0
SEND0
DATA
EP0
RESET0
count
parity
37
8
9
10
11
0
3
0
92 - 137
0 - 7
DEC