

LDL06E05A

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1 論理譜

```
logicname LDL06E05A

entity main
input RESET;
input SCLK;
input SIN;
input TAKE;
output Q[8];
output SET;

bitr en;
bitr sp[2];
bitr count[5];
bitr no[4];
bitr cp[2];
bitr data[10];
bitr set;
bitn count7p;
bitn count15p;
{
output TOP[2]; TOP=sp;
output T1P[5]; T1P=count;
output T2P; T2P=en;
output T3P[2]; T3P=cp;
}
Q=data.1:8;
SET=set;

if (RESET)
sp=0;
else
if (SCLK)
switch(sp)
case 0: sp=1;
case 1: sp=2;
default: sp=sp;
endswitch
else
sp=0;
endif
endif

if (RESET)
count=0;
else
if (sp.0)
if (SIN)
if (en)
if (count15p)
count=0;
else
count=count+1;
endif
else
count=0;
endif
else
if (en)
if (count15p)
count=0;
else
count=count+1;
endif
else
if (count7p)
count=0;
else
count=count+1;
endif
endif
endif
else
count=count;
endif
endif

switch(count)
case 7: count7p=1;
case 15: count15p=1;
endswitch

if (count15p)
switch(cp)
case 0: cp=1;
case 1: cp=2;
default: cp=cp;
endswitch
else
```

```

        cp=0;
    endif
    if (RESET|set)
        en=0;
    else
        if (count7p)
            if (sp.0)
                en=1;
            else
                en=en;
            endif
        else
            if (TAKE)
                en=0;
            else
                en=en;
            endif
        endif
    endif
endif

if (RESET)
    no=0;
else
    if (en)
        if (cp.0)
            no=no+1;
        else
            no=no;
        endif
    else
        no=0;
    endif
endif

if (RESET)
    set=0;
else
    switch(no)
        case 8: set=1;
        default:
            if (TAKE)
                set=0;
            else
                set=set;
            endif
        endif
    endswitch
endif

if (cp.0)
    data.0=SIN;
        data.1:9=data.0:8;
    else
        data=data;
    endif
endif

ende

entity sim
output RESET;
output SCLK;
output SIN;
output TAKE;
output Q[8];
output SET;

bitr tc[10];
bitr sd;

part main(RESET,SCLK,SIN,TAKE,Q,SET)

tc=tc+1;

SCLK=tc.1;
SIN=sd;

if (tc<5) RESET=1; endif

switch(tc)
    case 2: sd=1;
    case 10: sd=0; { START BIT }
    case 74: sd=1; { DATA 0 }
    case 138: sd=0; { DATA 1 }
    case 202: sd=1; { DATA 2 }
    case 266: sd=0; { DATA 3 }
    case 330: sd=1; { DATA 4 }
    case 394: sd=0; { DATA 5 }
    case 458: sd=1; { DATA 6 }
    case 522: sd=0; { DATA 7 }
    case 586: sd=1; { STOP BIT }
    default: sd=sd;
endswitch

switch(tc)
    case 620: TAKE=1;
endswitch

ende

endlogic

```

2 動作

図 1 動作 (1/13)

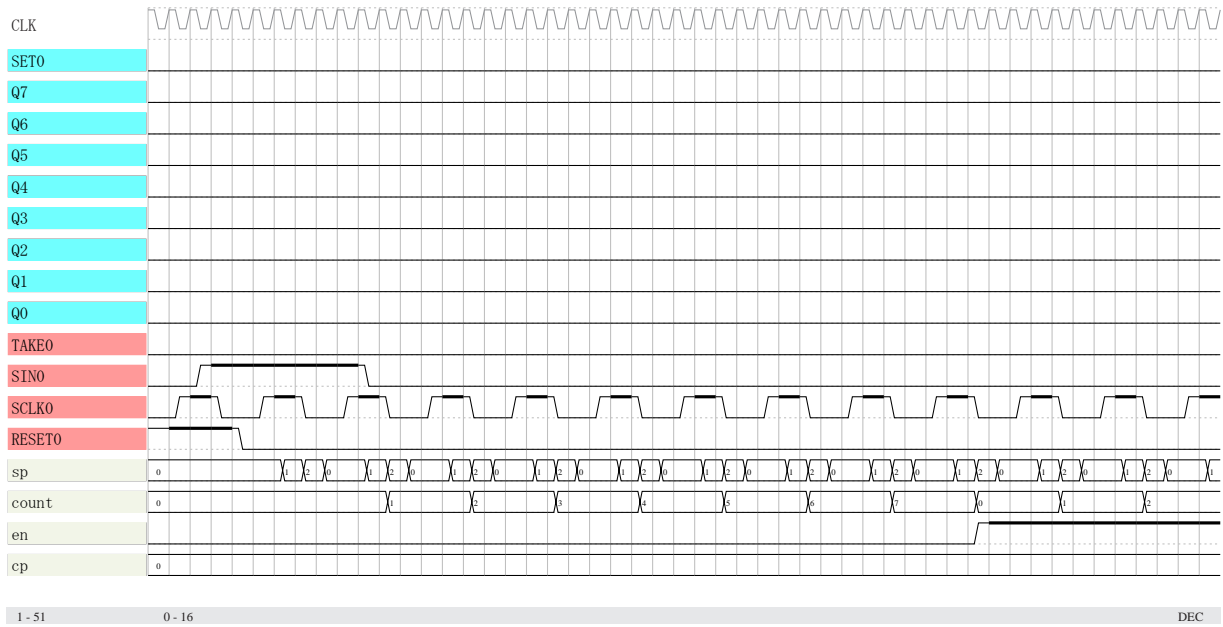


図 2 動作 (2/13)

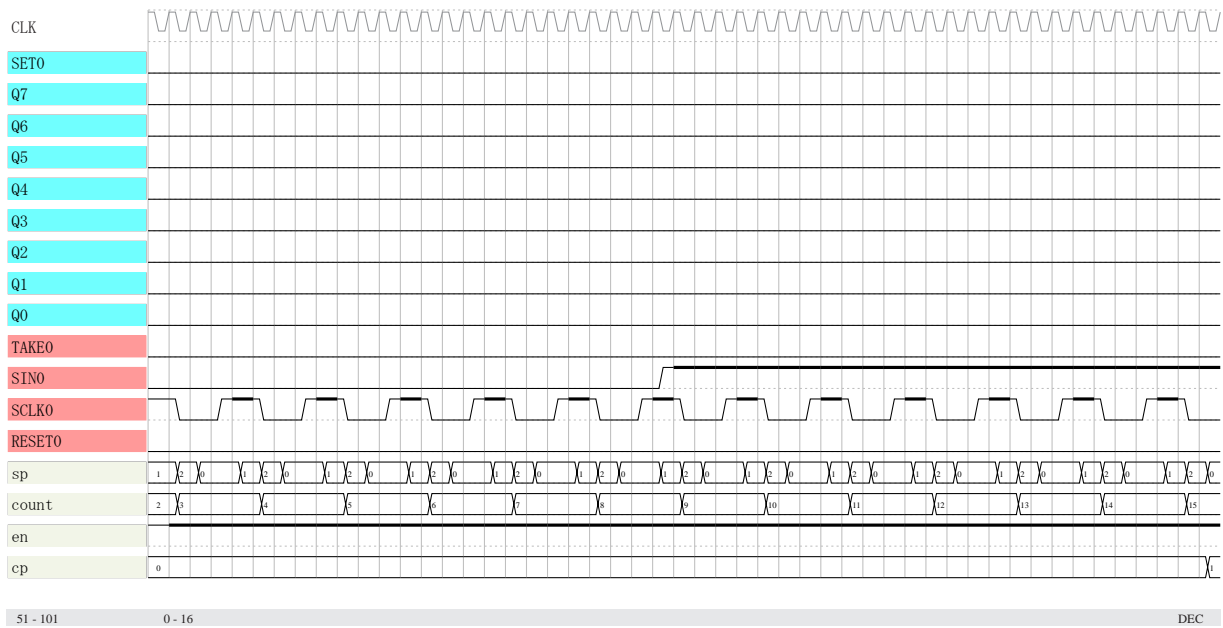


図3 動作 (3/13)

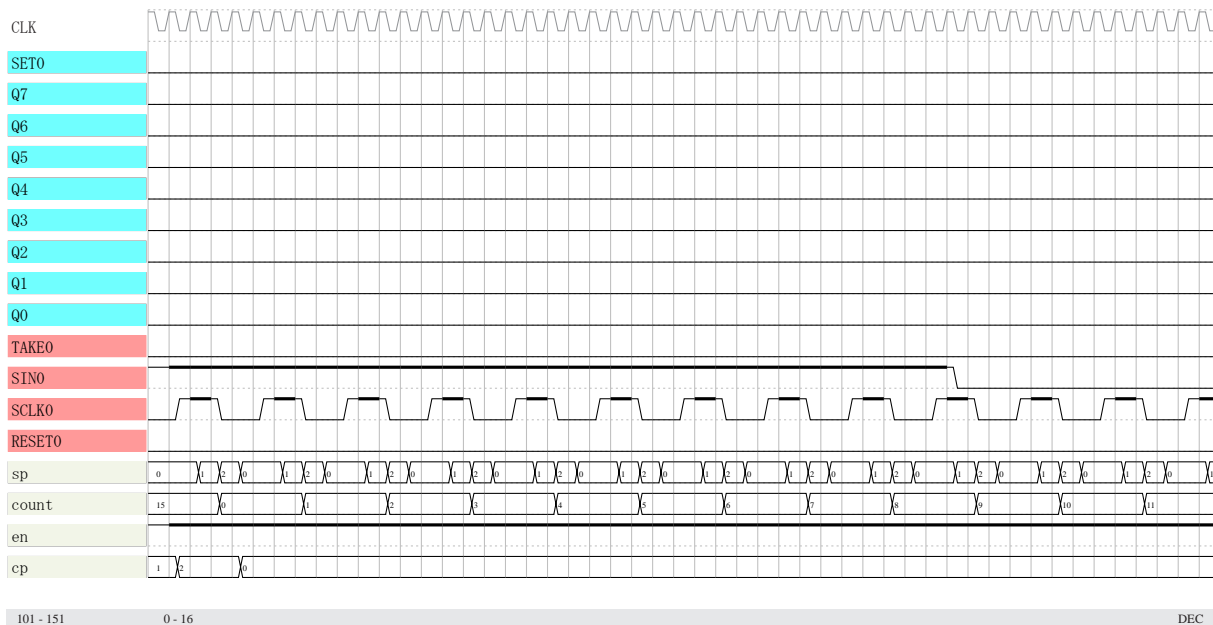


図4 動作 (4/13)

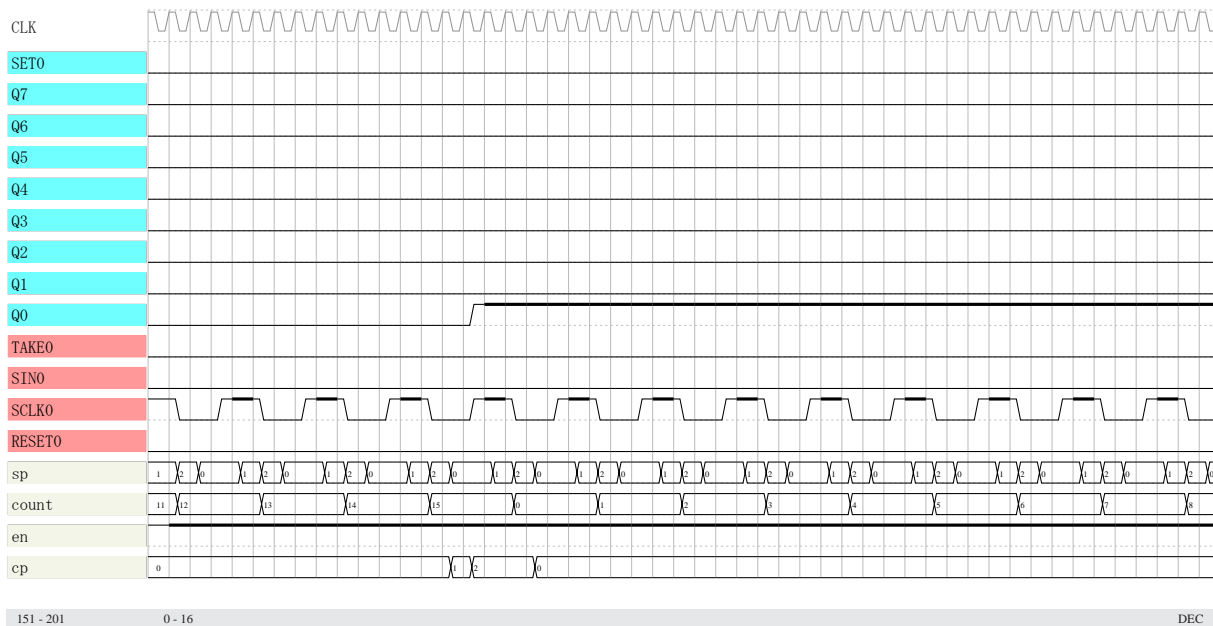


図 5 動作 (5/13)

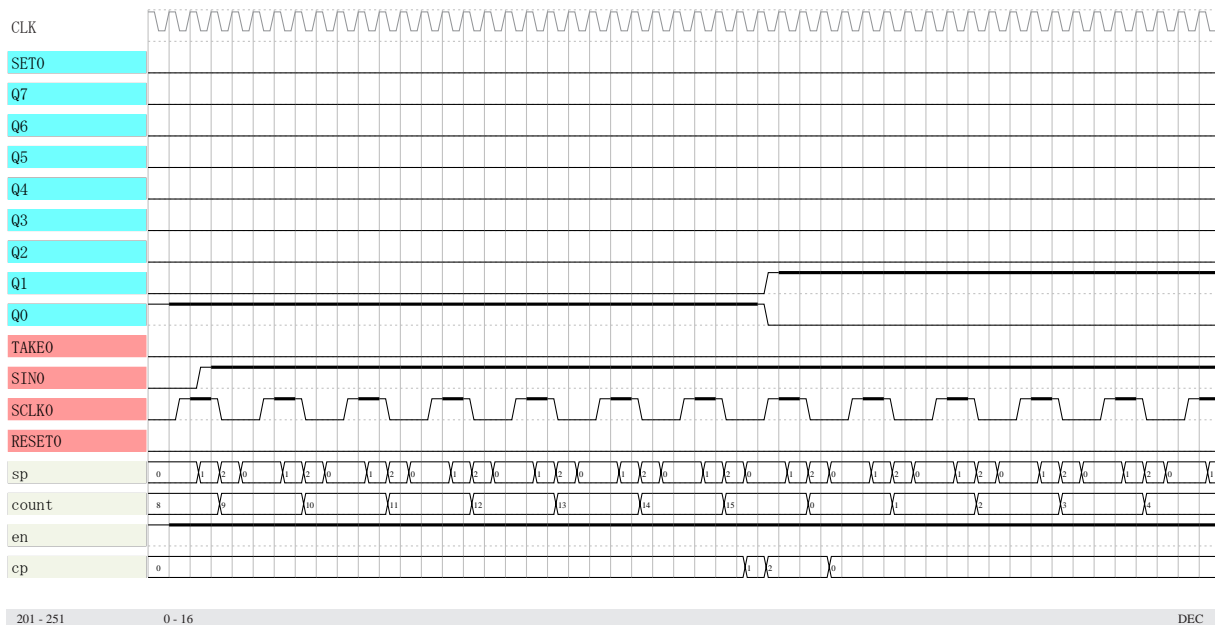


図 6 動作 (6/13)

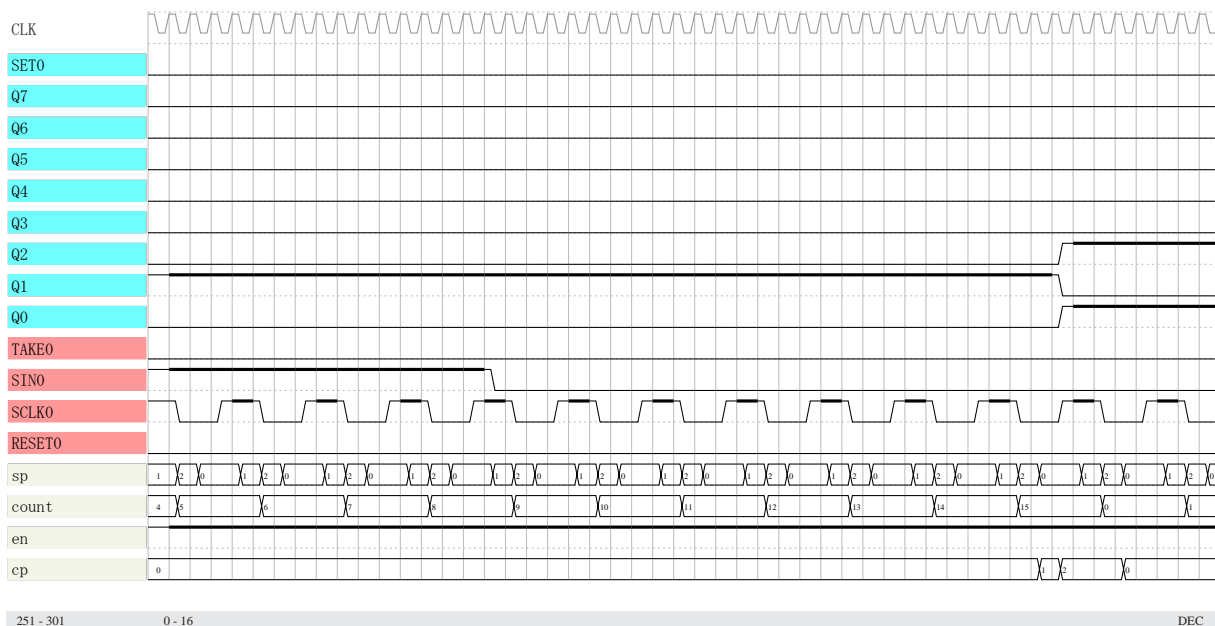


図7 動作 (7/13)

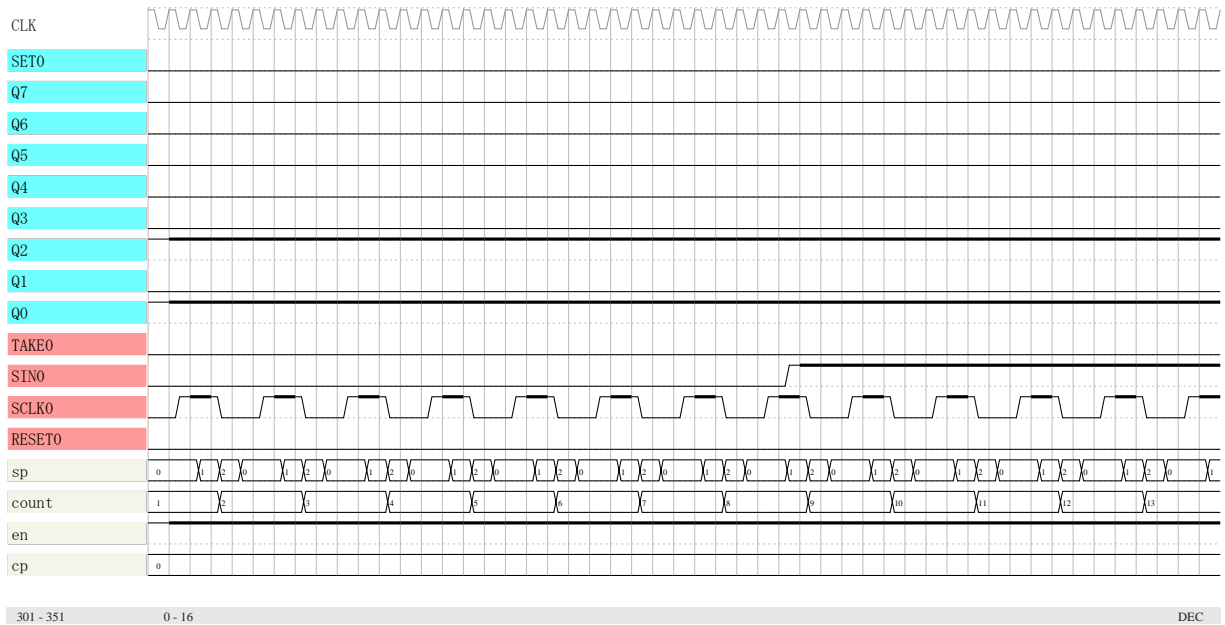


図8 動作 (8/13)

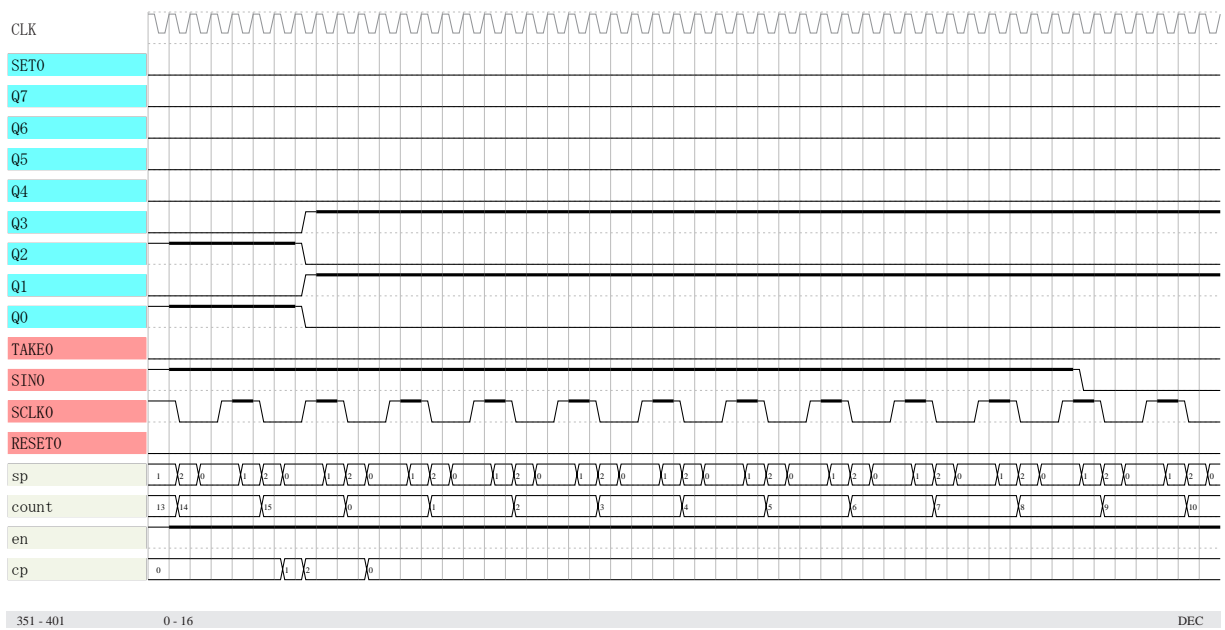


図 9 動作 (9/13)

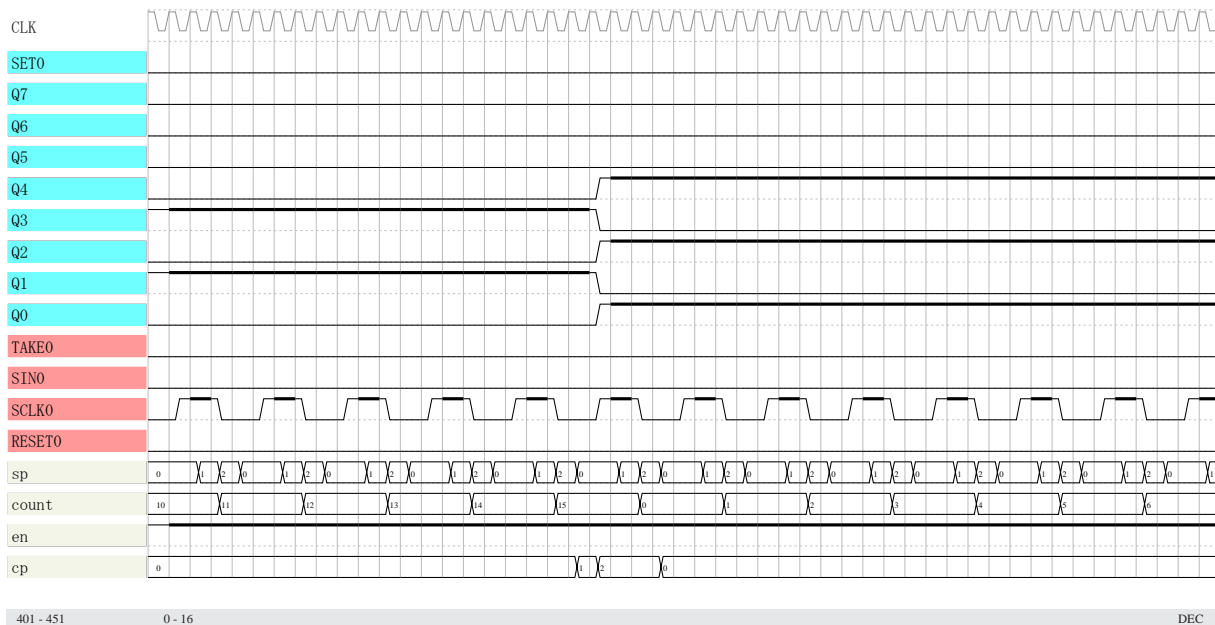


図 10 動作 (10/13)

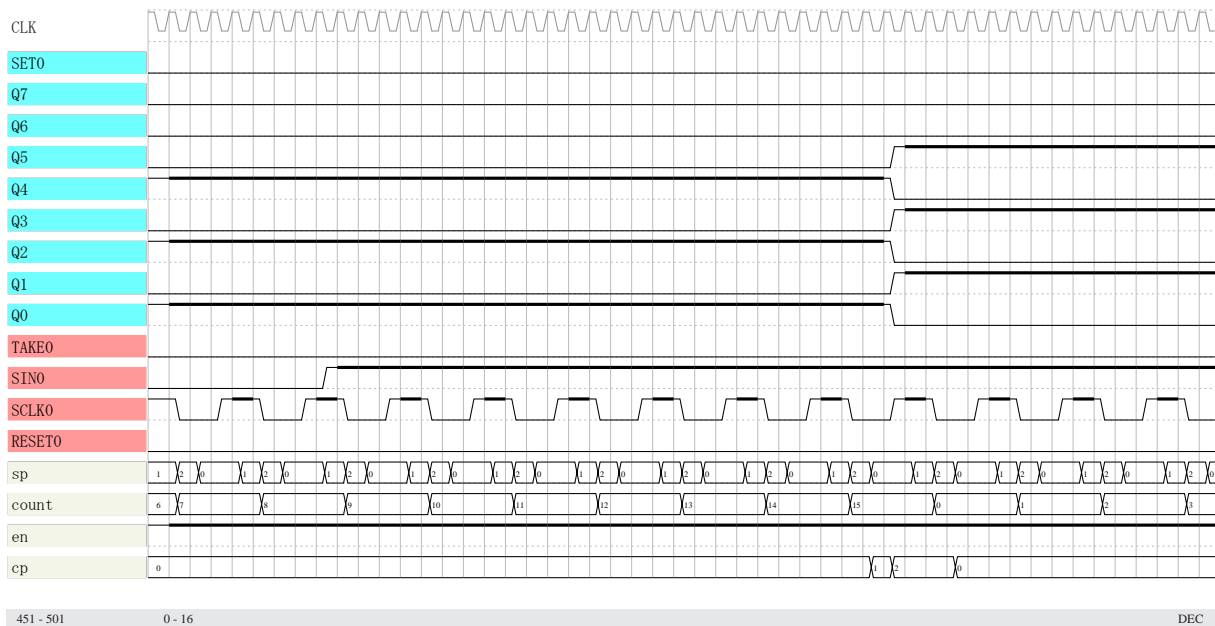


図 11 動作 (11/13)

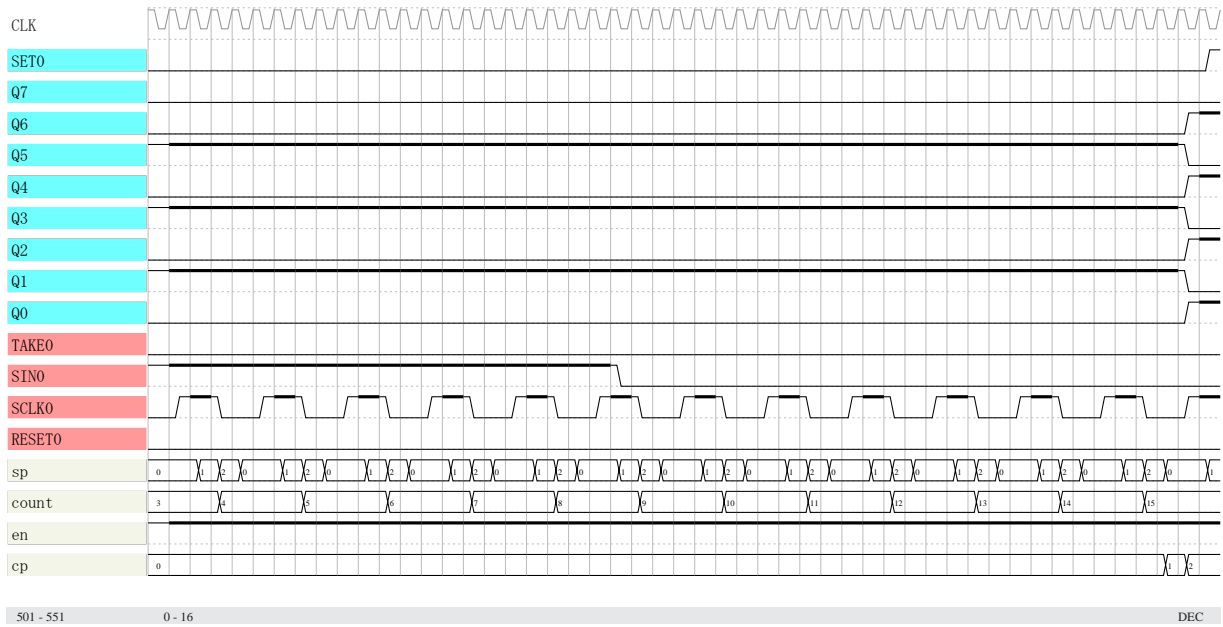


図 12 動作 (12/13)

