LDL06E12A

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1　論理譜

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logicname LDL06E12A

procedure MEMORY
input  RESET;
input  CS;
input  WP;
input  DATAIN[4];
output DATAOUT[4];

bitr memory[4];

   DATAOUT=memory;

   if (RESET)
      memory=0;
   else
      if (WP)
         if (CS)
            memory=DATAIN;
         else
            memory=memory;
         endif
      else
         memory=memory;
      endif
   endif
endp

entity main
input RESET;
input ADDA[3];
input ADDB[3];
input ADDC[3];
input DATAIN[4];
input WP;
output DATABOUT[4];
output DATACOUT[4];

bitn memory0[4];
bitn memory1[4];
bitn memory2[4];
bitn memory3[4];
bitn memory4[4];
bitn memory5[4];
bitn memory6[4];
bitn memory7[4];
bitn ADDA0p;
bitn ADDA1p;
bitn ADDA2p;
bitn ADDA3p;
bitn ADDA4p;
bitn ADDA5p;
bitn ADDA6p;
bitn ADDA7p;

   switch(ADDB)
      case 0: DATABOUT=memory0;
      case 1: DATABOUT=memory1;
      case 2: DATABOUT=memory2;
      case 3: DATABOUT=memory3;
      case 4: DATABOUT=memory4;
      case 5: DATABOUT=memory5;
      case 6: DATABOUT=memory6;
      case 7: DATABOUT=memory7;
   endswitch

   switch(ADDC)
      case 0: DATACOUT=memory0;
      case 1: DATACOUT=memory1;
      case 2: DATACOUT=memory2;
      case 3: DATACOUT=memory3;
      case 4: DATACOUT=memory4;
      case 5: DATACOUT=memory5;
      case 6: DATACOUT=memory6;
      case 7: DATACOUT=memory7;
   endswitch

   memory0=MEMORY(RESET,ADDA0p,WP,DATAIN);
   memory1=MEMORY(RESET,ADDA1p,WP,DATAIN);
   memory2=MEMORY(RESET,ADDA2p,WP,DATAIN);
   memory3=MEMORY(RESET,ADDA3p,WP,DATAIN);
   memory4=MEMORY(RESET,ADDA4p,WP,DATAIN);
   memory5=MEMORY(RESET,ADDA5p,WP,DATAIN);
   memory6=MEMORY(RESET,ADDA6p,WP,DATAIN);
   memory7=MEMORY(RESET,ADDA7p,WP,DATAIN);

   switch(ADDA)
      case 0: ADDA0p=1;
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      case 1: ADDA1p=1;
      case 2: ADDA2p=1;
      case 3: ADDA3p=1;
      case 4: ADDA4p=1;
      case 5: ADDA5p=1;
      case 6: ADDA6p=1;
      case 7: ADDA7p=1;
   endswitch

ende

entity sim
output RESET;
output ADDA[3];
output ADDB[3];
output ADDC[3];
output DATAIN[4];
output WP;
output DATABOUT[4];
output DATACOUT[4];

bitr tc[8];

   part main(RESET,ADDA,ADDB,ADDC
            ,DATAIN,WP
            ,DATABOUT,DATACOUT)

      tc=tc+1;

      if (tc<5) RESET=1; endif

      switch(tc)
         case 10: ADDA=0; DATAIN=10; WP=1;
         case 11: ADDA=1; DATAIN=11; WP=1;
         case 12: ADDA=2; DATAIN=12; WP=1;
         case 13: ADDA=3; DATAIN=13; WP=1;
         case 14: ADDA=4; DATAIN=14; WP=1;
         case 15: ADDA=5; DATAIN=15; WP=1;
         case 16: ADDA=6; DATAIN=9; WP=1;
         case 17: ADDA=7; DATAIN=8; WP=1;
         case 20: ADDB=1; ADDC=7;
         case 21: ADDB=2; ADDC=6;
         case 22: ADDB=3; ADDC=5;
         case 23: ADDB=4; ADDC=4;
         case 24: ADDB=5; ADDC=3;
         case 25: ADDB=6; ADDC=2;
         case 26: ADDB=7; ADDC=1;
      endswitch

   ende

   endlogic
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2 動作

図 1 動作