

# LDL06E25A

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## 1 論理譜

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logicname LDL06E25A

procedure MEMORY
input  RESET;
input  CS;
input  WP;
input  DATAIN[4];
output DATAOUT[4];

bitr memory[4];

    DATAOUT=memory;

    if (RESET)
        memory=0;
    else
        if (WP)
            if (CS)
                memory=DATAIN;
            else
                memory=memory;
            endif
        else
            memory=memory;
        endif
    endif
endp

entity main
input RESET;
input ADDA[3];
input ADDB[3];
input DATAIN[4];
input WP;
output DATAAOUT[4];
output DATABOOUT[4];

bitn memory0[4];
bitn memory1[4];
bitn memory2[4];
bitn memory3[4];
bitn memory4[4];
bitn memory5[4];
bitn memory6[4];

bitn memory7[4];
bitr wp[2];

switch(ADDA)
    case 0: DATAAOUT=memory0;
    case 1: DATAAOUT=memory1;
    case 2: DATAAOUT=memory2;
    case 3: DATAAOUT=memory3;
    case 4: DATAAOUT=memory4;
    case 5: DATAAOUT=memory5;
    case 6: DATAAOUT=memory6;
    case 7: DATAAOUT=memory7;
endswitch

switch(ADDB)
    case 0: DATABOOUT=memory0;
    case 1: DATABOOUT=memory1;
    case 2: DATABOOUT=memory2;
    case 3: DATABOOUT=memory3;
    case 4: DATABOOUT=memory4;
    case 5: DATABOOUT=memory5;
    case 6: DATABOOUT=memory6;
    case 7: DATABOOUT=memory7;
endswitch

memory0=MEMORY(RESET,1,wp.0,DATAIN);
memory1=MEMORY(RESET,1,wp.0,memory0);
memory2=MEMORY(RESET,1,wp.0,memory1);
memory3=MEMORY(RESET,1,wp.0,memory2);
memory4=MEMORY(RESET,1,wp.0,memory3);
memory5=MEMORY(RESET,1,wp.0,memory4);
memory6=MEMORY(RESET,1,wp.0,memory5);
memory7=MEMORY(RESET,1,wp.0,memory6);

if (RESET)
    wp=0;
else
    switch(wp)
        case 0:
            if (WP) wp=1; endif
        case 1:
            if (WP) wp=2; else wp=0; endif
        default:
            if (WP) wp=wp; else wp=0; endif
    endswitch
endif
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        endswitch
    endif
ende

entity sim
output RESET;
output ADDA[3];
output ADDB[3];
output DATAIN[4];
output WP;
output DATAAOUT[4];
output DATABOUT[4];

bitr tc[8];

    part main(RESET,ADDA,ADDB,DATAIN,WP
        ,DATAAOUT,DATABOUT)

    tc=tc+1;

    if (tc<5) RESET=1; endif

    switch(tc)
        case 10: DATAIN=10; WP=1;
        case 11: DATAIN=10; WP=0;
        case 12: DATAIN=11; WP=1;
        case 13: DATAIN=11; WP=0;
        case 14: DATAIN=12; WP=1;
        case 15: DATAIN=12; WP=0;
        case 16: DATAIN=14; WP=1;
        case 17: DATAIN=14; WP=0;
        case 18: DATAIN=15; WP=1;
        case 19: DATAIN=15; WP=0;
        case 20: DATAIN=9; WP=1;
        case 21: DATAIN=9; WP=0;
        case 22: DATAIN=8; WP=1;
        case 23: DATAIN=8; WP=0;
        case 24: DATAIN=7; WP=1;
        case 25: DATAIN=7; WP=0;
        case 30: ADDB=1; ADDA=7;
        case 31: ADDB=2; ADDA=6;
        case 32: ADDB=3; ADDA=5;
        case 33: ADDB=4; ADDA=4;
        case 34: ADDB=5; ADDA=3;
        case 35: ADDB=6; ADDA=2;
        case 36: ADDB=7; ADDA=1;
    endswitch
endlogic

```

## 2 動作

図 1 動作

