LDL06E26A

LDLABO

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1 論理譜

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logicname LDL06E26A

library LDL06E04A   { キーボード }
library LDL06E09A   { 表示器 }
library LDL06E25A   { メモリ }

entity main
input  RESET;
input  SCLK;
input  YIN[5];
input  ADD[3];
input  TAKE;

output XSEL[5];
output SEGOUT[7];
output KETAOUT[8];
output DATA[4];
output SET;

bitn keyb[12];
bitn dsp[18];
bitn memory[8];
bitn keydata[6];
bitn dspdata[4];
bitn setkey;
bitn takekey;
bitn data[4];
bitn adda[3];
bitn addb[3];
bitn memclr;
bitr set;
bitn memset;

{
output TOP; TOP=setkey;
output T1P[4]; T1P=data;
output T2P[6]; T2P=keydata;
}

   XSEL=keyb.7:11;
   SEGOUT=dsp.0:6;
   KETAOUT=dsp.7:14;
   DATA=memory.4:7;
SET=set;

addb=ADD;

keyb=LDL06E04A(RESET,SCLK,YIN,takekey);

keyb.12=1;
keydata=keyb.0:5;
setkey=keyb.6;
takekey=keyb.6;

dsp=LDL06E09A(RESET,SCLK,dspdata);

dsp.18=1;
adda=dsp.15:17;

memory=LDL06E25A(memclr,adda,addb,data,memset);

memory.8=1;
dspdata=memory.0:3;

switch(keydata)
   case 0x24: data=0;
   case 0x23: data=1;
   case 0x1b: data=2;
   case 0x13: data=3;
   case 0x22: data=4;
   case 0x1a: data=5;
   case 0x12: data=6;
   case 0x21: data=7;
   case 0x19: data=8;
   case 0x11: data=9;
   from:
      if (setkey) memset=1; endif
endswitch

if (RESET)
   memclr=1;
else
   switch(keydata)
      case 0x1c: memclr=1;
   endswitch
endif
```

```
   if (RESET)
      set=0;
   else
      if (setkey)
         switch(keydata)
            case 0x14: set=1;
            default: set=set;
         endswitch
      else
         if (TAKE)
            set=0;
         else
            set=set;
         endif
      endif
   endif

ende

entity sim
output RESET;
output SCLK;
output YIN[5];
output ADD[3];
output TAKE;
output XSEL[5];
output SEGOUT[7];
output KETAOUT[8];
output DATA[4];
output SET;

bitr tc[12];

   part main(RESET,SCLK,YIN,ADD,TAKE
            ,XSEL,SEGOUT,KETAOUT
            ,DATA,SET)

   tc=tc+1;

   if (tc<5) RESET=1; endif

   SCLK=tc.4;

   switch(tc)
      case 145:  YIN.3=1; { 1 を押す }
      case 146:  YIN.3=1;

      case 273:  YIN.3=1; { 2 を押す }
      case 274:  YIN.3=1;

      case 401:  YIN.3=1; { 3 を押す }
      case 402:  YIN.3=1;

      case 465:  YIN.2=1; { 4 を押す }
      case 466:  YIN.2=1;

      case 593:  YIN.2=1; { 5 を押す }
      case 594:  YIN.2=1;

      case 721:  YIN.2=1; { 6 を押す }
      case 722:  YIN.2=1;

      case 785:  YIN.1=1; { 7 を押す }
      case 786:  YIN.1=1;

      case 913:  YIN.1=1; { 8 を押す }
      case 914:  YIN.1=1;
{
      case 1041:  YIN.1=1; { 9 を押す }
      case 1042:  YIN.1=1;
}
      case 1201:  YIN.4=1; { RET を押す }
      case 1202:  YIN.4=1;

      case 1393:  YIN.4=1; { CLR を押す }
      case 1394:  YIN.4=1;

   endswitch

   switch(tc)
      case 1250: ADD=0;
      case 1251: ADD=1;
      case 1252: ADD=2;
      case 1253: ADD=3;
      case 1254: ADD=4;
      case 1255: ADD=5;
      case 1256: ADD=6;
      case 1257: ADD=7;
   endswitch

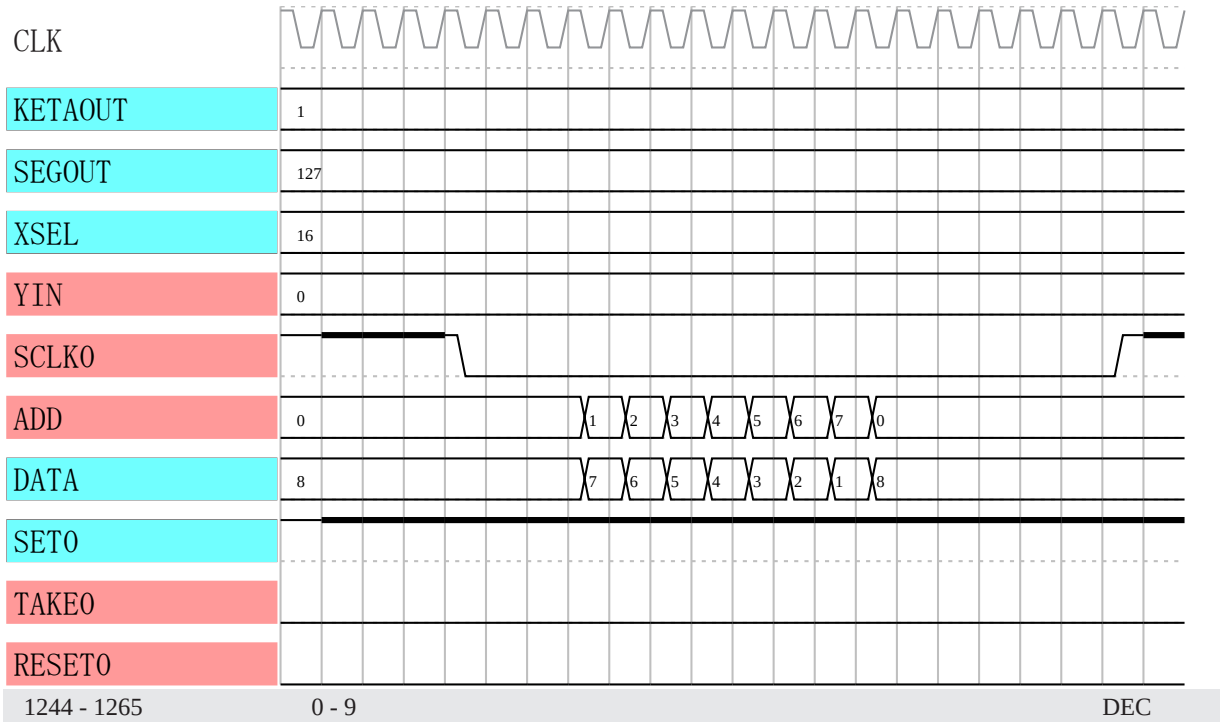
   switch(tc)
      case 1270: TAKE=1;
   endswitch

ende

endlogic
```

2 動作

図 1　動作


CLK
KETAOUT
1
SEGOUT
127
XSEL
16
YIN
0
SCLKO
ADD
0
1
2
3
4
5
6
7
0
DATA
8
7
6
5
4
3
2
1
8
SETO
TAKEO
RESETO
1244 - 1265
0 - 9
DEC