LDL06E27A

LDLABO

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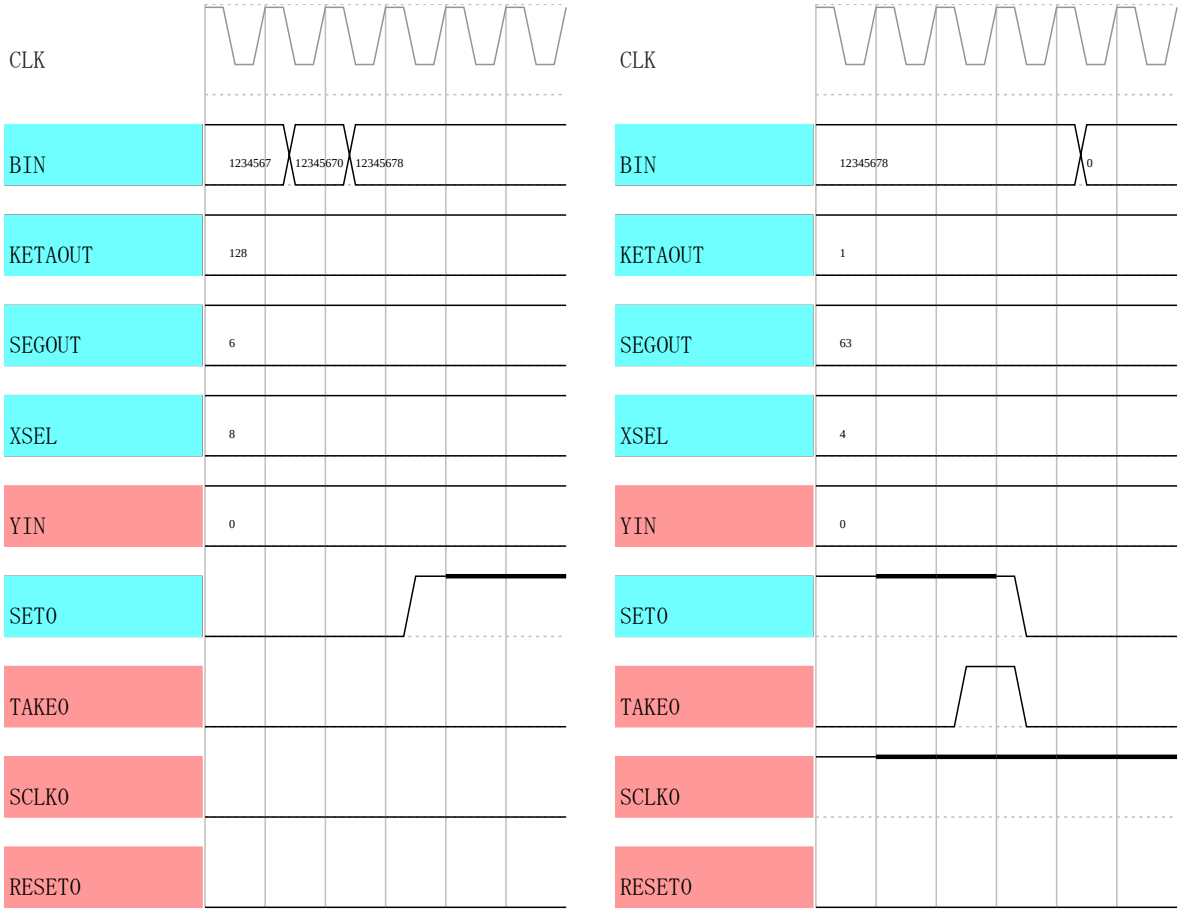
1 論理譜

```
logicname LDL06E27A

library LDL06E26A  { 端末 }
library LDL06E21A  { 変換器 }

entity main
input  RESET;
input  SCLK;
input  YIN[5];
input  ADD[3];
input  TAKE;

output XSEL[5];
output SEGOUT[7];
output KETAOUT[8];
output BIN[32];
output SET;

bitn term[25];
bitn change[36];
bitn data[4];
bitn add[3];
bitn take;
bitr setseq[2];
bitn changereset;
bitn set;

   BIN=change.0:31;
   SET=setseq.1;

   term=LDL06E26A(RESET,SCLK,YIN,add,take);

   term.25=1;
   XSEL=term.0:4;
   SEGOUT=term.5:11;
   KETAOUT=term.12:19;
   data=term.20:23;
   set=term.24;

   change=LDL06E21A(changereset,data);

   change.36=1;
   add=change.32:34;
   take=change.35;

   if (RESET)
      setseq=0;
   else
      switch(setseq)
         case 0:
            if (set) setseq=1; endif
         case 1:
            if (take)
               setseq=2;
            else
               setseq=setseq;
            endif
         case 2:
            if (TAKE)
               setseq=0;
            else
               setseq=setseq;
            endif
      endswitch
   endif

   switch(setseq)
      case 1: changereset=0;
      case 2: changereset=0;
      default: changereset=1;
   endswitch

ende

entity sim
output RESET;
output SCLK;
output YIN[5];
output ADD[3];
output TAKE;
output XSEL[5];
output SEGOUT[7];
output KETAOUT[8];
output BIN[32];
output SET;

bitr tc[12];
```

```
part main(RESET,SCLK,YIN,ADD,TAKE,XSEL
         ,SEGOUT,KETAOUT,BIN,SET)

tc=tc+1;

if (tc<5) RESET=1; endif

SCLK=tc.4;

switch(tc)
   case 145:  YIN.3=1; { 1 を押す }
   case 146:  YIN.3=1;

   case 273:  YIN.3=1; { 2 を押す }
   case 274:  YIN.3=1;

   case 401:  YIN.3=1; { 3 を押す }
   case 402:  YIN.3=1;

   case 465:  YIN.2=1; { 4 を押す }
   case 466:  YIN.2=1;

   case 593:  YIN.2=1; { 5 を押す }
   case 594:  YIN.2=1;

   case 721:  YIN.2=1; { 6 を押す }
   case 722:  YIN.2=1;

   case 785:  YIN.1=1; { 7 を押す }
   case 786:  YIN.1=1;

   case 913:  YIN.1=1; { 8 を押す }
   case 914:  YIN.1=1;

   case 1201:  YIN.4=1; { RET を押す }
   case 1202:  YIN.4=1;

   case 1393:  YIN.4=1; { CLR を押す }
   case 1394:  YIN.4=1;

   case 1500:  TAKE=1;
   endswitch

ende

endlogic
```

2 動作

図 1　動作



1219 - 1224	0 - 8	DEC

1498 - 1503	0 - 8	DEC