LDL06E31A

LDLABO

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1 論理譜

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logicname LDL06E27A

library LDL06E30A  { 端末 }
library LDL06E21A  { 変換器 }

entity main
input  RESET;
input  SCLK;
input  YIN[5];

output XSEL[5];
output SEGOUT[7];
output KETAOUT[8];
output ANS[32];
output EOP;

bitn term[28];
bitn change[36];
bitn data[4];
bitn add[3];
bitr take;
bitr setseq[3];
bitn changereset;
bitn set;
bitn func[3];
bitr calcseq[4];
bitr calcop[3];
bitn opend;
bitr regA[32];
bitr regB[32];
bitn bin[32];
bitr execop[3];
bitn changecomplete;
bitr answer[32];
bitr eop;


output T0P[4];   T0P=calcseq;
output T1P;      T1P=set;
output T2P[3];   T2P=func;
output T3P;      T3P=take;
output T4P[32];  T4P=bin;
output T5P[32];  T5P=regA;
output T6P[3];   T6P=calcop;
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output T7P[3];   T7P=execop;
output T8P[32];  T8P=regB;
output T9P[3];   T9P=setseq;
output T10P[32]; T10P=answer;


   ANS=answer;
   EOP=eop;

   bin=change.0:31;

   term=LDL06E30A(RESET,SCLK,YIN,add,take);

   term.28=1;
   XSEL=term.0:4;
   SEGOUT=term.5:11;
   KETAOUT=term.12:19;
   data=term.20:23;
   set=term.24;
   func=term.25:27;

   change=LDL06E21A(changereset,data);

   change.36=1;
   add=change.32:34;
   changecomplete=change.35;

   if (RESET)
      setseq=0;
   else
      switch(setseq)
         case 0:
            if (set) setseq=1; endif   { 端末数値確定 }
         case 1:
            if (take)
               setseq=2;               { BCD を BIN に変換終了 }
            else
               setseq=setseq;          { BCD を BIN に変換中 }
            endif
         case 2:
            switch(calcseq)
               case 2:  setseq=4;
               default: setseq=setseq;
            endswitch
         case 4:
            if (set)
               setseq=setseq;
            else
               setseq=0;
            endif
      endswitch
   endif

   if (RESET)
      take=0;
   else
      switch(take)
         case 0:
            if (changecomplete) take=1; endif
         case 1:
            if (set)
               take=take;
            else
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            take=0;
         endif
   endswitch
endif

switch(setseq)
   case 1: changereset=0;
   case 2: changereset=0;
   default: changereset=1;
endswitch

if (RESET)
   calcseq=0;
else
   switch(calcseq)
      case 0:       { 数値入力を待つ }
         if (set)
            calcseq=1;
         else
            calcseq=calcseq;
         endif

      case 1:       { BCD から BIN に変換中 }
         if (setseq.1)
            calcseq=2;
         else
            calcseq=calcseq;
         endif

      case 2:       { 端末の初期化を待つ }
         if (set)
            calcseq=calcseq;
         else
            calcseq=3;
         endif

      case 3:       { 計算の実行 }
         if (opend)
            calcseq=4;
         else
            calcseq=calcseq;
         endif

      case 4:       { 終了処理 }
         calcseq=5;

      case 5:       { 終了 }
         calcseq=0;
   endswitch
endif

if (RESET)
   calcop=0;
else
   if (set)
      switch(func)
         case 1: calcop=1;   { RET }
         case 2: calcop=2;   { *   }
         case 3: calcop=3;   { /   }
         case 4: calcop=4;   { +   }
         case 5: calcop=5;   { -   }
      endswitch
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   else
      calcop=calcop;
   endif
endif

if (RESET)
   execop=0;
else
   switch(calcseq)
      case 1:
         switch(execop)
            case 1:  execop=calcop;
            default: execop=execop;
         endswitch
      case 4:  execop=calcop;
      default: execop=execop;
   endswitch
endif

if (RESET)
   regB=0;
else
   if (setseq.1)
      regB=bin;
   else
      switch(calcseq)
         case 4:  regB=0;
         default: regB=regB;
      endswitch
   endif
endif

if (RESET)
   regA=0;
else
   switch(calcseq)
      case 4:
         switch(execop)
            case 0: regA=regB;
            case 4: regA=answer;   { 加算結果を記憶 }
         endswitch
      default: regA=regA;
   endswitch
endif

switch(execop)
   case 0: opend=1;
   case 4: opend=answer.32;
endswitch

switch(execop)
   case 4: answer=regA+regB;
endswitch

if (RESET)
   eop=0;
else
   switch(calcseq)
      case 4:
         switch(execop)
            case 0:  eop=0;
            default: eop=1;
         endswitch
```

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      endswitch
   endif

ende

entity sim
output RESET;
output SCLK;
output YIN[5];
output XSEL[5];
output SEGOUT[7];
output KETAOUT[8];
output ANS[32];
output EOP;

bitr tc[12];

   part main(RESET,SCLK,YIN,XSEL,SEGOUT,KETAOUT,ANS,EOP)

   tc=tc+1;

   if (tc<5) RESET=1; endif

   SCLK=tc.4;

   switch(tc)
      case 145:  YIN.3=1; { 1 を押す }
      case 146:  YIN.3=1;

      case 273:  YIN.3=1; { 2 を押す }
      case 274:  YIN.3=1;

      case 401:  YIN.3=1; { 3 を押す }
      case 402:  YIN.3=1;

      case 465:  YIN.2=1; { 4 を押す }
      case 466:  YIN.2=1;

      case 593:  YIN.2=1; { 5 を押す }
      case 594:  YIN.2=1;

      case 721:  YIN.2=1; { 6 を押す }
      case 722:  YIN.2=1;

      case 785:  YIN.1=1; { 7 を押す }
      case 786:  YIN.1=1;

      case 913:  YIN.1=1; { 8 を押す }
      case 914:  YIN.1=1;

      case 1169:  YIN.3=1; { + を押す }
      case 1170:  YIN.3=1;

      case 1393:  YIN.4=1; { CLR を押す }
      case 1394:  YIN.4=1;

      case 1521:  YIN.1=1; { 9 を押す }
      case 1522:  YIN.1=1;

      case 1585:  YIN.4=1; { 0 を押す }
      case 1586:  YIN.4=1;

      case 1745:  YIN.3=1; { 1 を押す }
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      case 1746:  YIN.3=1;

      case 1873:  YIN.3=1; { 2 を押す }
      case 1874:  YIN.3=1;

      case 2001:  YIN.3=1; { 3 を押す }
      case 2002:  YIN.3=1;

      case 2065:  YIN.2=1; { 4 を押す }
      case 2066:  YIN.2=1;

      case 2193:  YIN.2=1; { 5 を押す }
      case 2194:  YIN.2=1;

      case 2321:  YIN.2=1; { 6 を押す }
      case 2322:  YIN.2=1;

      case 2481:  YIN.4=1; { = を押す }
      case 2482:  YIN.4=1;

      case 2545:  YIN.1=1; { 7 を押す }
      case 2546:  YIN.1=1;

      case 2609:  YIN.3=1; { + を押す }
      case 2610:  YIN.3=1;

   endswitch

ende

endlogic
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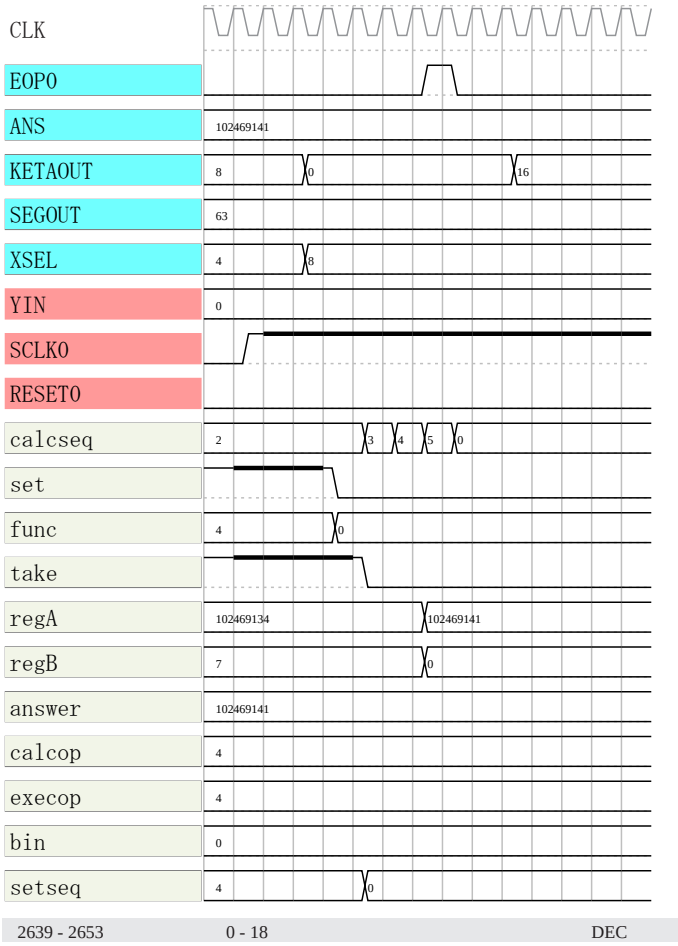
2 動作

図 1　動作


CLK
EOPO
ANS
102469141
KETAOUT
8
0
16
SEGOUT
63
XSEL
4
8
YIN
0
SCLKO
RESETO
calcseq
2
3
4
5
0
set
func
4
0
take
regA
102469134
102469141
regB
7
0
answer
102469141
calcop
4
execop
4
bin
0
setseq
4
0
2639 - 2653
0 - 18
DEC