LDL06F04B

LDLABO

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1 論理譜

```
logicname LDL06F04B

entity main
input  reset;
input  a[32];
input  b[32];
input  sel;
output y[32];
output ready;

bitr   p[64];
bitr   q[32];
bitn   c[33];
bitn   np[33];
bitn   nb[33];
bitr   count[6];
bitn   stop;

   np.0:31=p.32:63;
   nb.0:31=b;

   if (reset)
      p.0:31=a;
   else
      if (stop)
         p=p;
      else
         if (c.32)
            p.1:63=p.0:62;
         else
            p.33:63=c.0:30;
            p.1:32=p.0:31;
         endif
      endif
   endif

   c=np-nb;

   if (reset)
      q=0;
   else
      if (stop)
         q=q;
      else
         if (c.32)
            q.1:31=q.0:30;
         else
            q.0=1;
            q.1:31=q.0:30;
         endif
      endif
   endif

   if (reset)
      count=0;
   else
      if (stop)
         count=count;
      else
         count=count+1;
      endif
   endif

   if (count==33) stop=1; endif

   if (sel)
      y=np.1:32;
   else
      y=q;
   endif

   ready=stop;

ende

entity sim
output reset;
output a[32];
output b[32];
output sel;
output y[32];
output ready;

bitr   tc[8];

   part main(reset,a,b,sel,y,ready)

   tc=tc+1;
```

```
if (tc<5) reset=1; endif
if (tc==105) reset=1; endif

if (tc<100)
   a=12345678;
   b=90;
else
   a=98765432;
   b=11;
endif

if (tc>50) sel=1; endif

ende

endlogic
```

2 動作

図 1　動作