LDL06F06A0

LDLABO

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1 論理譜

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logicname LDL06F06A0

library LDL06E04A0  { キーボード }
library LDL06E09A   { 表示器 }
library LDL06F02A   { メモリ }

entity main
input  RESET;
input  SCLK;
input  YIN[5];
input  ADD[3];
input  TAKE;
input  EXTADD[3];
input  EXTDATA[4];
input  EXTWP;

output XSEL[5];
output SEGOUT[7];
output KETAOUT[8];
output DATA[4];
output SET;
output FUNC[3];

bitn keyb[12];
bitn dsp[18];
bitn memory[8];
bitn keydata[6];
bitn dspdata[4];
bitn setkey;
bitn takekey;
bitn data[4];
bitn adda[3];
bitn addb[3];
bitn addc[3];
bitr memclr[2];
bitr set;
bitn memset;
bitr opcode[3];
bitn datacin[4];
bitn wcp;
bitr setkeyp[2];

output T0P;    T0P=setkey;
output T1P[4]; T1P=data;
output T2P[6]; T2P=keydata;
output T3P;    T3P=memset;
output T4P[2]; T4P=memclr;


   XSEL=keyb.7:11;
   SEGOUT=dsp.0:6;
   KETAOUT=dsp.7:14;
   DATA=memory.4:7;
   SET=set;
   FUNC=opcode;

   addb=ADD;

   keyb=LDL06E04A(RESET,SCLK,YIN,takekey);

   keyb.12=1;
   keydata=keyb.0:5;
   setkey=keyb.6;
   takekey=keyb.6;

   dsp=LDL06E09A(RESET,SCLK,dspdata);

   dsp.18=1;
   adda=dsp.15:17;

   memory=LDL06F02A(memclr.0,adda,addb,addc,data
                  ,datacin,memset,wcp);

   addc=EXTADD;
   datacin=EXTDATA;
   wcp=EXTWP;

   memory.8=1;
   dspdata=memory.0:3;

   switch(keydata)
      case 0x24: data=0;
      case 0x23: data=1;
      case 0x1b: data=2;
      case 0x13: data=3;
      case 0x22: data=4;
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   case 0x1a: data=5;
   case 0x12: data=6;
   case 0x21: data=7;
   case 0x19: data=8;
   case 0x11: data=9;
   from:
      if (setkeyp.0) memset=1; endif
endswitch

if (RESET)
   memclr=1;
else
   switch(memclr)
      case 0:
         if (TAKE)
            memclr=1;
         else
            switch(keydata)
               case 0x1c: memclr=1;
            endswitch
         endif
      case 1:
         memclr=2;
      case 2:
         switch(TAKE,keydata)
            case 0,0:    memclr=0;
            case 0,0x1c: memclr=memclr;
            case 1,0:    memclr=memclr;
            case 1,0x1c: memclr=memclr;
         endswitch
   endswitch
endif

if (RESET)
   set=0;
else
   if (setkey)
      switch(keydata)
         case 0x14: set=1;   { = }
         case 0x09: set=1;   { * }
         case 0x0a: set=1;   { / }
         case 0x0b: set=1;   { + }
         case 0x0c: set=1;   { - }
         default: set=set;
      endswitch
   else
      if (TAKE)
         set=0;
      else
         set=set;
      endif
   endif
endif

if (RESET)
   opcode=0;
else
   if (setkey)
      switch(keydata)
         case 0x14: opcode=1;
         case 0x09: opcode=2;
         case 0x0a: opcode=3;
         case 0x0b: opcode=4;
         case 0x0c: opcode=5;
         case 0x1c: opcode=0;
         default: opcode=opcode;
      endswitch
   else
      if (TAKE)
         opcode=0;
      else
         opcode=opcode;
      endif
   endif
endif

   if (RESET)
      setkeyp=0;
   else
      switch(setkeyp)
         case 0:
            if (setkey) setkeyp=1; endif
         case 1:
            setkeyp=2;
         case 2:
            if (setkey)
               setkeyp=setkeyp;
            else
               setkeyp=0;
            endif
      endswitch
   endif

ende

entity sim
output RESET;
output SCLK;
output YIN[5];
output ADD[3];
output TAKE;
output EXTADD[3];
output EXTDATA[4];
output EXTWP;
output XSEL[5];
output SEGOUT[7];
output KETAOUT[8];
output DATA[4];
output SET;
output FUNC[3];

bitr tc[12];

   part main(RESET,SCLK,YIN,ADD,TAKE
            ,EXTADD,EXTDATA,EXTWP
            ,XSEL,SEGOUT,KETAOUT
            ,DATA,SET,FUNC)

   tc=tc+1;

   if (tc<5) RESET=1; endif

   SCLK=tc.4;

   switch(tc)
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      case 145:  YIN.3=1; { 1 を押す }
      case 146:  YIN.3=1;

      case 273:  YIN.3=1; { 2 を押す }
      case 274:  YIN.3=1;

      case 401:  YIN.3=1; { 3 を押す }
      case 402:  YIN.3=1;

      case 465:  YIN.2=1; { 4 を押す }
      case 466:  YIN.2=1;

      case 593:  YIN.2=1; { 5 を押す }
      case 594:  YIN.2=1;

      case 721:  YIN.2=1; { 6 を押す }
      case 722:  YIN.2=1;

      case 785:  YIN.1=1; { 7 を押す }
      case 786:  YIN.1=1;

      case 913:  YIN.1=1; { 8 を押す }
      case 914:  YIN.1=1;
{
      case 1041:  YIN.1=1; { 9 を押す }
      case 1042:  YIN.1=1;
}
      case 1201:  YIN.4=1; { RET を押す }
      case 1202:  YIN.4=1;

      case 1393:  YIN.4=1; { CLR を押す }
      case 1394:  YIN.4=1;

   endswitch

   switch(tc)
      case 1250: ADD=0;
      case 1251: ADD=1;
      case 1252: ADD=2;
      case 1253: ADD=3;
      case 1254: ADD=4;
      case 1255: ADD=5;
      case 1256: ADD=6;
      case 1257: ADD=7;
   endswitch

   switch(tc)
      case 1270: TAKE=1;
   endswitch
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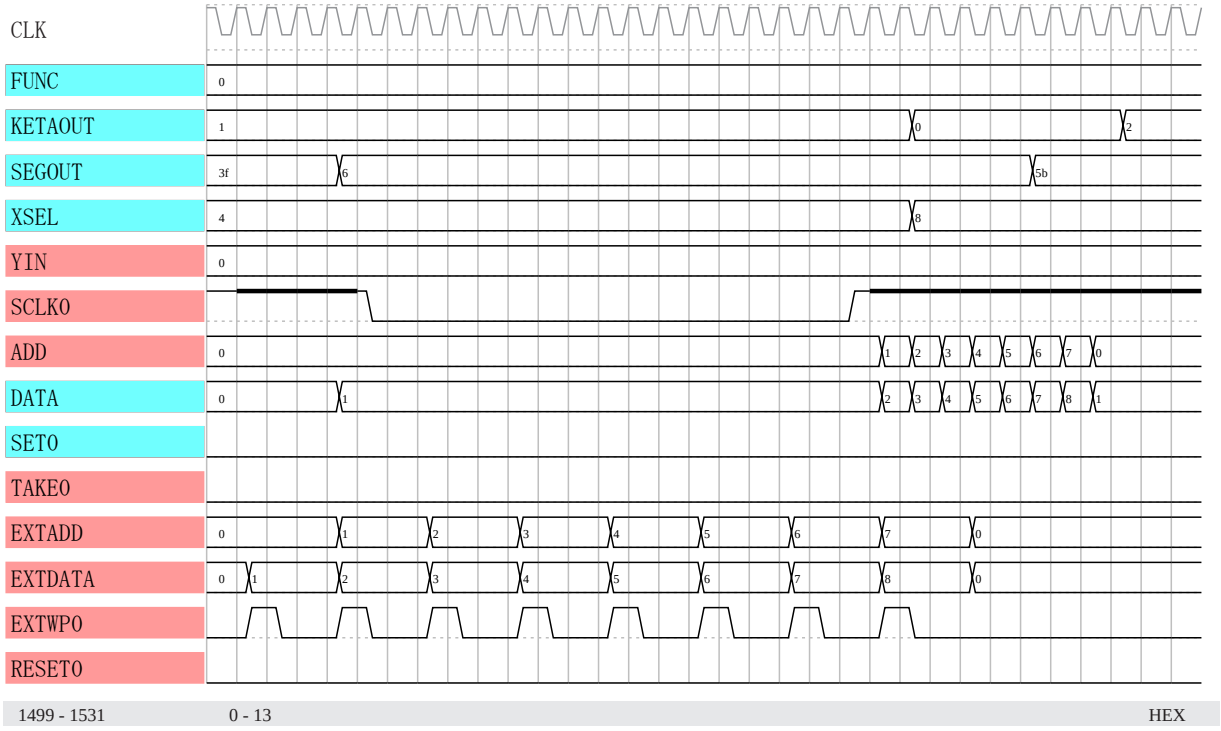
```
   switch(tc)
      case 1500: EXTADD=0; EXTDATA=1; EXTWP=1;
      case 1501: EXTADD=0; EXTDATA=1;
      case 1502: EXTADD=0; EXTDATA=1;

      case 1503: EXTADD=1; EXTDATA=2; EXTWP=1;
      case 1504: EXTADD=1; EXTDATA=2;
      case 1505: EXTADD=1; EXTDATA=2;

      case 1506: EXTADD=2; EXTDATA=3; EXTWP=1;
      case 1507: EXTADD=2; EXTDATA=3;
      case 1508: EXTADD=2; EXTDATA=3;

      case 1509: EXTADD=3; EXTDATA=4; EXTWP=1;
      case 1510: EXTADD=3; EXTDATA=4;
      case 1511: EXTADD=3; EXTDATA=4;

      case 1512: EXTADD=4; EXTDATA=5; EXTWP=1;
      case 1513: EXTADD=4; EXTDATA=5;
      case 1514: EXTADD=4; EXTDATA=5;

      case 1515: EXTADD=5; EXTDATA=6; EXTWP=1;
      case 1516: EXTADD=5; EXTDATA=6;
      case 1517: EXTADD=5; EXTDATA=6;

      case 1518: EXTADD=6; EXTDATA=7; EXTWP=1;
      case 1519: EXTADD=6; EXTDATA=7;
      case 1520: EXTADD=6; EXTDATA=7;

      case 1521: EXTADD=7; EXTDATA=8; EXTWP=1;
      case 1522: EXTADD=7; EXTDATA=8;
      case 1523: EXTADD=7; EXTDATA=8;

   endswitch

   switch(tc)
      case 1520: ADD=0;
      case 1521: ADD=1;
      case 1522: ADD=2;
      case 1523: ADD=3;
      case 1524: ADD=4;
      case 1525: ADD=5;
      case 1526: ADD=6;
      case 1527: ADD=7;
   endswitch

ende

endlogic
```

2 動作

図 1　動作


CLK
FUNC
KETAOUT
SEGOUT
XSEL
YIN
SCLKO
ADD
DATA
SETO
TAKEO
EXTADD
EXTDATA
EXTWPO
RESETO
1499 - 1531
0 - 13
HEX